

**TESTING FOR THE VERIFICATION OF COMPLIANCE OF  
PV INVERTER WITH :  
ENGINEERING RECOMMENDATION G99 ISSUE 1-  
AMENDMENT 3, 16 MAY 2018,  
REQUIREMENTS FOR THE CONNECTION OF  
GENERATION EQUIPMENT IN PARALLEL WITH PUBLIC  
DISTRIBUTION NETWORKS ON OR AFTER 27 APRIL 2019**

Test Report Number ..... : GZES201203548901

Type .....



Tested Model..... : SOFAR 136KTL-HV

Variant Models ..... : SOFAR 75KTL; SOFAR 80KTL;  
SOFAR 100KTL; SOFAR 110KTL;  
SOFAR 100KTL-HV; SOFAR 125KTL-HV

**APPLICANT**

Hired by ..... : Shenzhen SOFARSOLAR Co., Ltd.  
401, Building 4, AnTongDa Industrial Park, District 68,  
Address ..... : XingDong Community, XinAn Street, BaoAn District,  
Shenzhen, Guangdong, China.

**TESTING LABORATORY**

Name ..... : SGS-CSTC Standards Technical Services Co., Ltd.  
Guangzhou Branch

Address ..... : 198 Kezhu Road, Science City, Economic & Technology  
Development Area, Guangzhou, Guangdong, China

Conducted (tested) by ..... : Hugo Zhang  
(Project Engineer)



*Hugo Zhang*

Approved by ..... : Roger Hu  
(Technical Reviewer)

*Roger Hu*

Date of issue..... : 20 / 03 / 2021

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**Test Report Historical Revision:**

Test Report Version	Date	Resume
GZES201203548901	20 / 03 / 2021	First issuance

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## 1 SCOPE

SGS-CSTC Standards Technical Services Co., Ltd. Guangzhou Branch has been contract by Shenzhen SOFAR SOLAR Co., Ltd, in order to perform the testing according the "ENGINEERING RECOMMENDATION G99 ISSUE 1-AMENDMENT 3, 16 MAY 2018, REQUIREMENTS FOR THE CONNECTION OF GENERATION EQUIPMENT IN PARALLEL WITH PUBLIC DISTRIBUTION NETWORKS ON OR AFTER 27 APRIL 2019".

Note: This standard details connection process, technical and compliance requirements for Type A, Type B, Type C and Type D Power Generating Modules. The tests offered at this test report evaluate the EUT compliance with the requirements of **Type A** defined as below:

### Type A

A Power Generating Module with a Connection Point below 110 kV and a Registered Capacity of 0.8 kW or greater but less than 1 MW.

### Type B

A Power Generating Module with a Connection Point below 110 kV and Registered Capacity of 1 MW or greater but less than 10 MW.

### Type C

A Power Generating Module with a Connection Point below 110 kV and a Registered Capacity of 10 MW or greater but less than 50 MW.

### Type D

A Power Generating Module with a Connection Point at or greater than 110 kV, and/or with a Registered Capacity of 50 MW or greater.

## 2 GENERAL INFORMATION

### 2.1 TESTING PERIOD AND CLIMATIC CONDITIONS

The necessary testing has been performed along between the 24<sup>th</sup> December of 2020 and 21<sup>st</sup> of January to 16<sup>th</sup> of March of 2021.


All the tests and checks have been performed at  $25 \pm 5^{\circ}\text{C}$ ,  $96 \text{ kPa} \pm 10 \text{ kPa}$  and  $50\% \text{ RH} \pm 10\% \text{ RH}$ ).

### SITE TEST

Name .....: Shenzhen SOFARSOLAR Co., Ltd.  
 Address .....: 401, Building 4, AnTongDa Industrial Park, District 68,  
 XingDong Community, XinAn Street, BaoAn District,  
 Shenzhen, Guangdong, China.

### 2.2 EQUIPMENT UNDER TESTING

Apparatus type .....: Solar Grid-tied Inverter (Three Phase)  
 Installation .....: Fixed(permanent connection)  
 Manufacturer .....: Shenzhen SOFARSOLAR Co., Ltd.  
 Address .....: 401, Building 4, AnTongDa Industrial Park, District 68,  
 XingDong Community, XinAn Street, BaoAn District,  
 Shenzhen, Guangdong, China.

Trade mark .....: 

Model / Type reference .....: **SOFAR 136KTL-HV**  
 Serial Number .....: SQ1EH1D6M1L005  
 Software Version .....: ARM V020010; DSPS V020010; DSPM V020010;  
 (DSPM is the main controller, DSPS is the sub-controller  
 and ARM is the communication control)

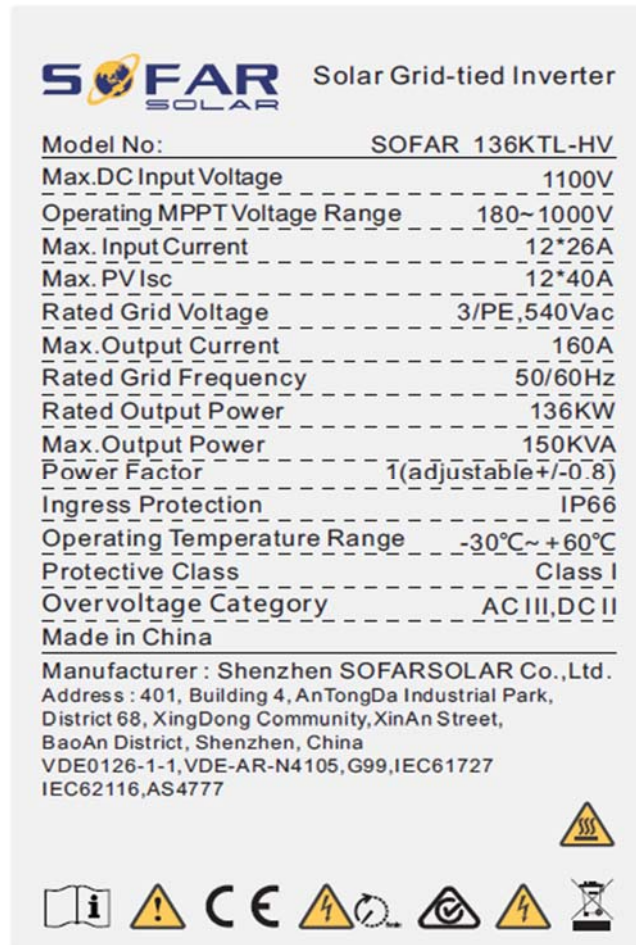
Rated Characteristics .....: DC input: 180-1000V<sub>MPPT</sub> (Max.1100V), 12\*26A  
 AC output: 3/PE 540Vac, 50Hz, 145A (Max.160A), 136KW

Date of manufacturing: 2020

Test item particulars

Input .....: DC  
 Output.....: AC  
 Class of protection against electric shock...: Class I  
 Degree of protection against moisture .....: IP66  
 Type of connection to the main supply .....: Three phase – Fixed installation  
 Cooling group .....: Fans  
 Modular .....: No  
 Internal Transformer.....: No

Copy of marking plate (representative):



Note:

1. The above markings are the minimum requirements required by the safety standard. For the final production samples, the additional markings which do not give rise to misunderstanding may be added.
2. Label is attached on the side surface of enclosure and visible after installation.
3. Labels of other models are as the same with SOFAR 136KTL-HV's except the parameters of rating.

**Equipment Under Testing:**

- SOFAR 136KTL-HV

**Variant models:**

- SOFAR 75KTL
- SOFAR 80KTL
- SOFAR 100KTL
- SOFAR 110KTL
- SOFAR 100KTL-HV
- SOFAR 125KTL-HV

The variants models have been included in this test report without tests because the following features don't change regarding to the tested model:

- Same connection system and hardware topology
- Same control algorithm.
- Output power within  $1/\sqrt{10}$  and 2 times of the rated output power or the EUT or Modular inverters.
- Same Firmware Version.

The models of SOFAR 75KTL, SOFAR 80KTL, SOFAR 100KTL, SOFAR 110KTL, SOFAR 100KTL-HV, SOFAR 125KTL-HV and SOFAR 136KTL-HV are identical on topological schematic circuit diagram and control solution codes except for the type designation, the input/output rating.

The models with suffix -HV means the output is 3/PE connection and the others are for 3/N/PE

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Following table shows the full ratings of the all models referenced in this report, marked in **bold letters** the ones subjected to testing:

Model	SOFAR 75KTL	SOFAR 80KTL	SOFAR 100KTL	SOFAR 110KTL	SOFAR 100KTL -HV	SOFAR 125KTL -HV	<b>SOFAR 136KTL -HV</b>
<b>DC Input</b>							
Max. DC voltage	1100V						
Rated input voltage	625V	625V	625V	625V	725V	725V	785V
Start-up operating voltage	200V						
MPPT voltage range	180V~1000V						
Full power MPPT voltage range	500V-850V				550V-850V		
Max. input current	8*26A	8*26A	10*26A	10*26A	10*26A	10*26A	12*26A
Max. input short circuit current	8*40A	8*40A	10*40A	10*40A	10*40A	10*40A	12*40A
<b>AC Output</b>							
Rated AC Output power (kW)	75kW	80kW	100kW	110kW	100kW	125kW	136kW
Max. AC Output power (kVA)	75kVA	88kVA	110kVA	121kVA	110kVA	137kVA	150kVA
Rated current	109A	116A	145A	159A	115A	144A	145A
Max. output current	113A	128A	160A	175A	128A	160A	160A
Nominal grid voltage	3/N/PE, 230V/400V				3/PE, 500V		3/PE, 540V
Nominal output frequency	50Hz						
Output power factor	1 default (adjustable +/-0.8)						
Operating temperature range	-30°C ~60°C						
Ingress protection	IP66						
Protective class	Class I						

The results obtained apply only to the particular sample tested that is the subject of the present test report. The most unfavorable result values of the verifications and tests performed are contained herein.

Throughout this report a point (comma) is used as the decimal separator.



### 2.3 MANUFACTURER AND FACTORY INFORMATION

Manufacturer Name..... : Shenzhen SOFARSOLAR Co., Ltd.

Manufacturer Address..... : 401, Building 4, AnTongDa Industrial Park,  
District 68, XingDong Community, XinAn Street,  
BaoAn District, Shenzhen, Guangdong, China

Factory Name..... : Dongguan SOFAR SOLAR Co., Ltd.

Factory Address..... : 1F - 6F, Building E, No. 1 JinQi Road, Bihu  
Industrial Park, Wulian Village, Fenggang Town,  
Dongguan, Guangdong, China.

**2.4 TEST EQUIPMENT LIST**

From 2020/12/24 to 2021/01/05:

From	No.	Equipment Name	Model No.	Equipment No.	Calibration Date	Equipment calibration due date
Sofar Solar	1	Digital oscilloscope	DSOX3014A	MY58491772	2020/01/14	2021/01/13
	2	Voltage probe	SI-9110	111152	2020/1/14	2021/1/13
	3	Voltage probe	SI-9110	152627	2020/01/14	2021/01/13
	4	Voltage probe	SI-9110	111134	2020/01/14	2021/01/13
	5	Current probe	CP1000A	C181000922	2020/01/14	2021/01/13
	6	Current probe	CP1000A	C181000925	2020/01/14	2021/01/13
	7	Current probe	CP1000A	C181000929	2020/01/14	2021/01/13
	8	Power analyzer	PA3000	PA3004-P0004-1422	2020/01/14	2021/01/13
	9	Power analyzer	PA5000H	C8202909082002110001	2020/03/02	2020/03/01
	10	Temperature & Humidity meter	TH101B	ZB-WSDJ-001	2020/01/14	2021/01/13
SGS	11	True RMS Multimeter	Fluke / 289C	GZE012-53	2020/02/21	2020/02/20

From 2021/01/06 to 2021/03/16:

From	No.	Equipment Name	Model No.	Equipment No.	Calibration Date	Equipment calibration due date
SofarSolar	1	Voltage probe	SI-9110	152655	2021/1/5	2022/1/4
	2	Voltage probe	SI-9110	111134	2021/1/5	2022/1/4
	3	Voltage probe	SI-9110	111539	2021/1/5	2022/1/4
	4	Current probe	CP1000A	C181000922	2021/1/5	2022/1/4
	5	Current probe	CP1000A	C181000929	2021/1/5	2022/1/4
	6	Current probe	CP1000A	C191000141	2021/1/5	2022/1/4
	7	Power analyzer	PA3000	C8202005651809220002	2021/1/5	2022/1/4
	8	Power analyzer	PA5000H	C8202909082002110002	2021/1/5	2022/1/4
	9	Temperature & Humidity meter	HTC-1	WSDJ-007	2020/12/28	2021/12/27
	10	Digital oscilloscope	DSOX3014T	MY59243036	2021/1/5	2022/1/4
SGS	11	True RMS Multimeter	Fluke / 187	GZE012-8	2020/12/04	2021/12/03

## 2.5 MEASUREMENT UNCERTAINTY

Associated uncertainties through measurements showed in this this report are the maximum allowable uncertainties.

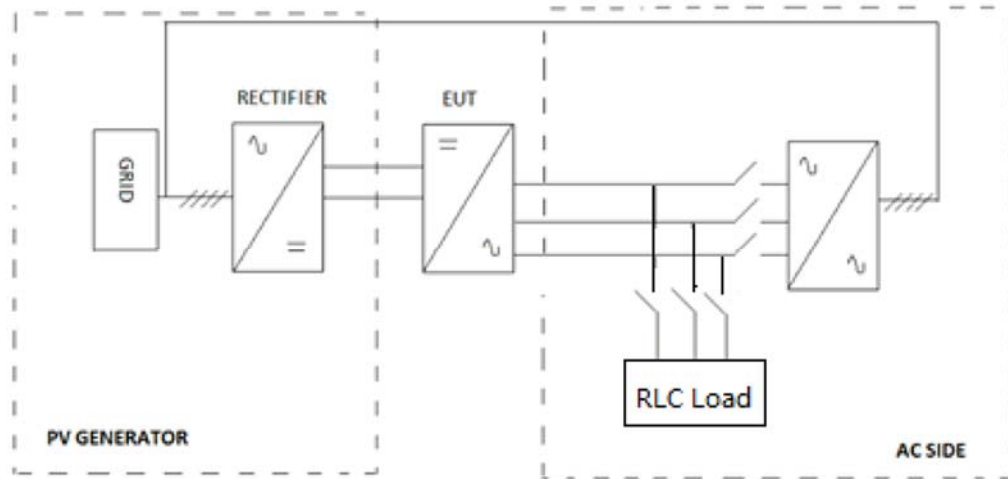
Magnitude	Uncertainty
Voltage measurement	$\pm 1.5 \%$
Current measurement	$\pm 2.0 \%$
Frequency measurement	$\pm 0.2 \%$
Time measurement	$\pm 0.2 \%$
Power measurement	$\pm 2.5 \%$
Phase Angle	$\pm 1^\circ$
Temperature	$\pm 3^\circ\text{C}$

Note1: Measurements uncertainties showed in this table are maximum allowable uncertainties. The measurement uncertainties associated with other parameters measured during the tests are in the laboratory at disposal of the petitioner.

Note2: Where the standard requires lower uncertainties that those in this table. Most restrictive uncertainty has been considered.

**2.6 TEST SET UP OF THE DIFFERENT STANDARD**

Below is the simplified construction of the test set up.



Different equipment has been used to take measures as it shows in chapter 2.3. Current and voltage clamps have been connected to the inverter input / output for all the tests. All the tests described in the following pages have used this specified test setup.

**The test bench used includes:**

<b>EQUIPMENT</b>	<b>MARK / MODEL</b>	<b>RATED CHARACTERISTICS</b>	<b>OWNER / ID.CODE</b>
AC source	Wogo / WLPA-33-1000kVA	1000 kVA 5-400 Vrms 44.5-65.5 Hz	--
DC source	Wogo / WDGC-1000kW	0 – 1500 Vdc (0.01 V step) 0 – 1333 A (0.01 A step)	--
RLC load	Qunlin / ACLT3816H	563.3kW, 563.3kVAr	--

## 2.7 Definitions

EUT	Equipment Under Testing	Hz	Hertz
A	Ampere	V	Volt
VA <sub>r</sub>	Volt-Ampere reactive	W	Watt
EMC	Electromagnetic Compatibility	p.u	Per unit
U <sub>n</sub>	Nominal Voltage	P <sub>n</sub>	Nominal Active Power
I <sub>n</sub>	Nominal Current	Q <sub>n</sub>	Nominal Reactive Power
I <sub>a</sub>	Active Current	S <sub>n</sub>	Nominal Apparent Power
I <sub>r</sub>	Reactive Current	THD	Total Harmonic Distortion
I <sub>h</sub>	Harmonic Current	TDD	Total Demand Distortion
PWHD	Partial Weighted Harmonic Distortion	PLT	Severity of Flicker Long-Term
PST	Severity of Flicker Short-Term	d(t)	Variation of Voltage
d <sub>max</sub>	Maximum Absolute Value of Voltage Variation	OV	Over Voltage
UV	Under Voltage	OF	Over Frequency
		UF	Under Frequency

### 3 RESUME OF TEST RESULTS

#### INTERPRETATION KEYS

Test object does meet the requirement ..... **P** Pass  
 Test object does not meet the requirement..... **F** Fails  
 Test case does not apply to the test object ..... **N/A** Not applicable  
 To make a reference to a table or an annex. .... See additional sheet  
 To indicate that the test has not been realized ..... **N/R** Not realized

STANDAARD CLAUSE	Report Clause	STANDARD REQUIREMENTS		RESULT
		G99 Issue 1 Amendment 3 May 2018		
		TEST	REMARKS	
Annex A 2-3 (1)	4.1	Operating Range		P
A.7.1.5	4.2.1	Harmonics		P
A.7.1.4.3	4.2.2	Voltage fluctuations and Flicker		P
A.7.1.4.4	4.2.3	DC injection		P
A.7.1.4.2	4.2.4	Power Factor		P
A.7.1.2.3	4.3.1	Frequency tests		P
A.7.1.2.2	4.3.2	Voltage tests:		P
A.7.1.2.4	4.3.3	Loss of Mains test		P
A.7.1.2.6	4.3.4	Loss of Mains Protection, Vector Shift Stability test.		P
		Loss of Mains Protection, RoCoF Stability test		P
A.7.1.3	4.4	Limited Frequency Sensitive Mode – Over frequency test		P
Annex A 2-3 (10)	4.5.1	Re-connection timer.		P
A.7.1.5	4.5.2	Fault level contribution		P
A.7.1.7	4.6	Self-Monitoring solid state switching	No solid state switching devices	N/A
Para 15.2.1	4.8	Wiring functional tests		N/A
Annex A 2-3 (14)	4.9	Logic Interface (input port)		P

## 4 TEST RESULTS

### 4.1 OPERATING RANGE

Two tests should be carried with the Power Generating Module operating at Registered Capacity and connected to a suitable test supply or grid simulation set. The power supplied by the primary source shall be kept stable within  $\pm 5\%$  of the apparent power value set for the entire duration of each test sequence.

Frequency, voltage and Active Power measurements at the output terminals of the Power Generating Module shall be recorded every second. The tests will verify that the Power Generating Module can operate within the required ranges for the specified period of time.

The Interface Protection shall be disabled during the tests.

The evaluation of this point has been made according to Annex A.7.2.2.

In case of a PV Power Park Module the PV primary source replaced by a DC source.

Test 1:

Voltage = 85% of nominal (195.5 V)

Frequency = 47 Hz

Power factor = 1

Period of test 20 s

Test 2:

Voltage = 85% of nominal (195.5 V)

Frequency = 47.5 Hz

Power factor = 1

Period of test 90 minutes

Test 3:

Voltage = 110% of nominal (253 V).

Frequency = 51.5 Hz

Power factor = 1

Period of test 90 minutes

Test 4:

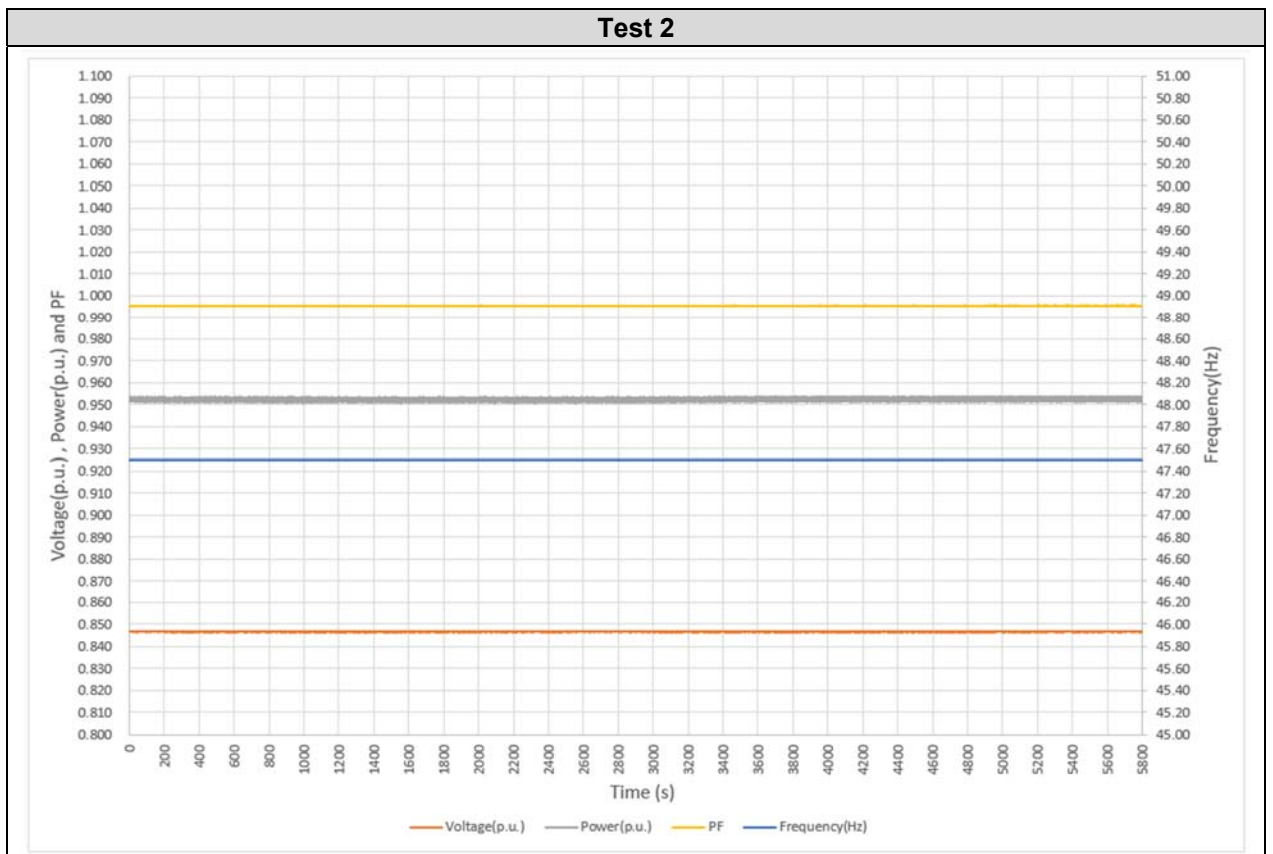
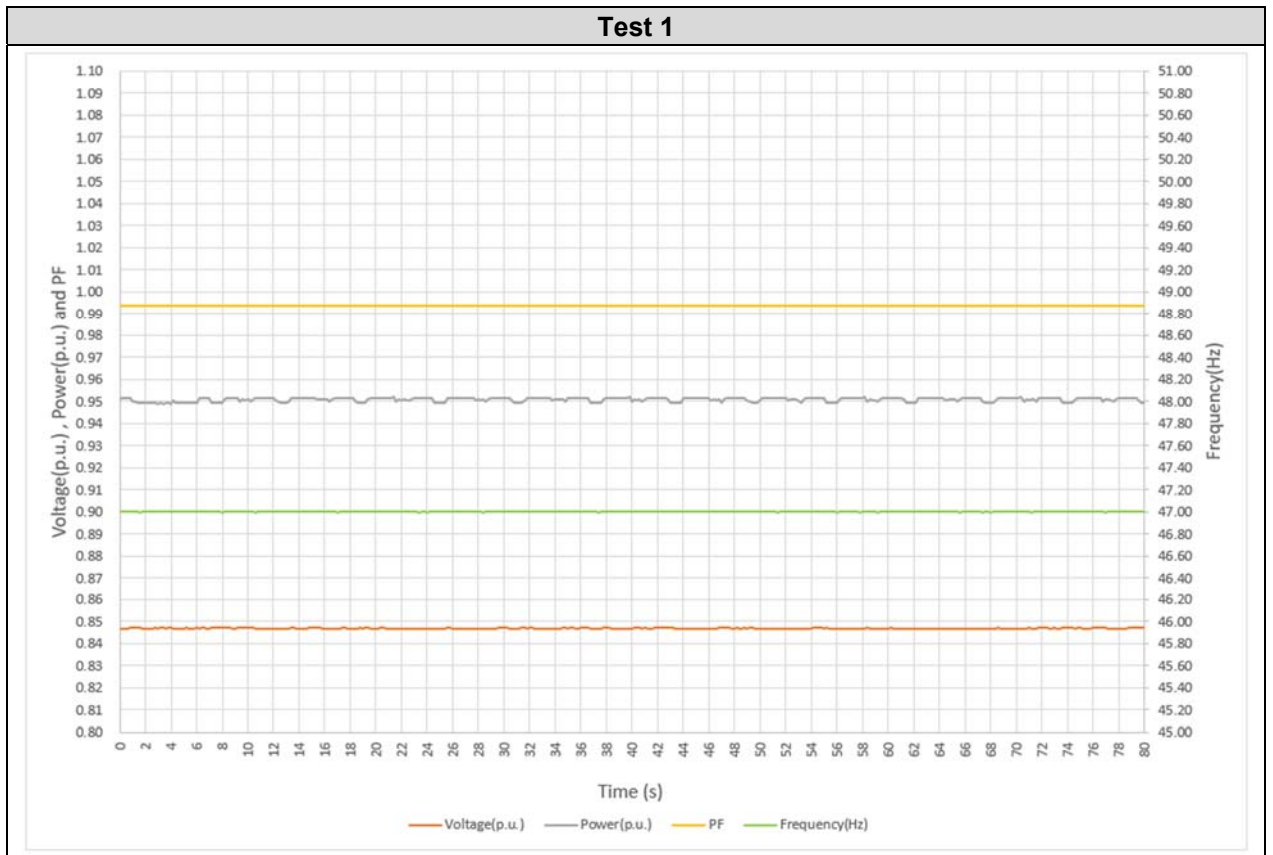
Voltage = 110% of nominal (253 V).

Frequency = 52.0 Hz

Power factor = 1

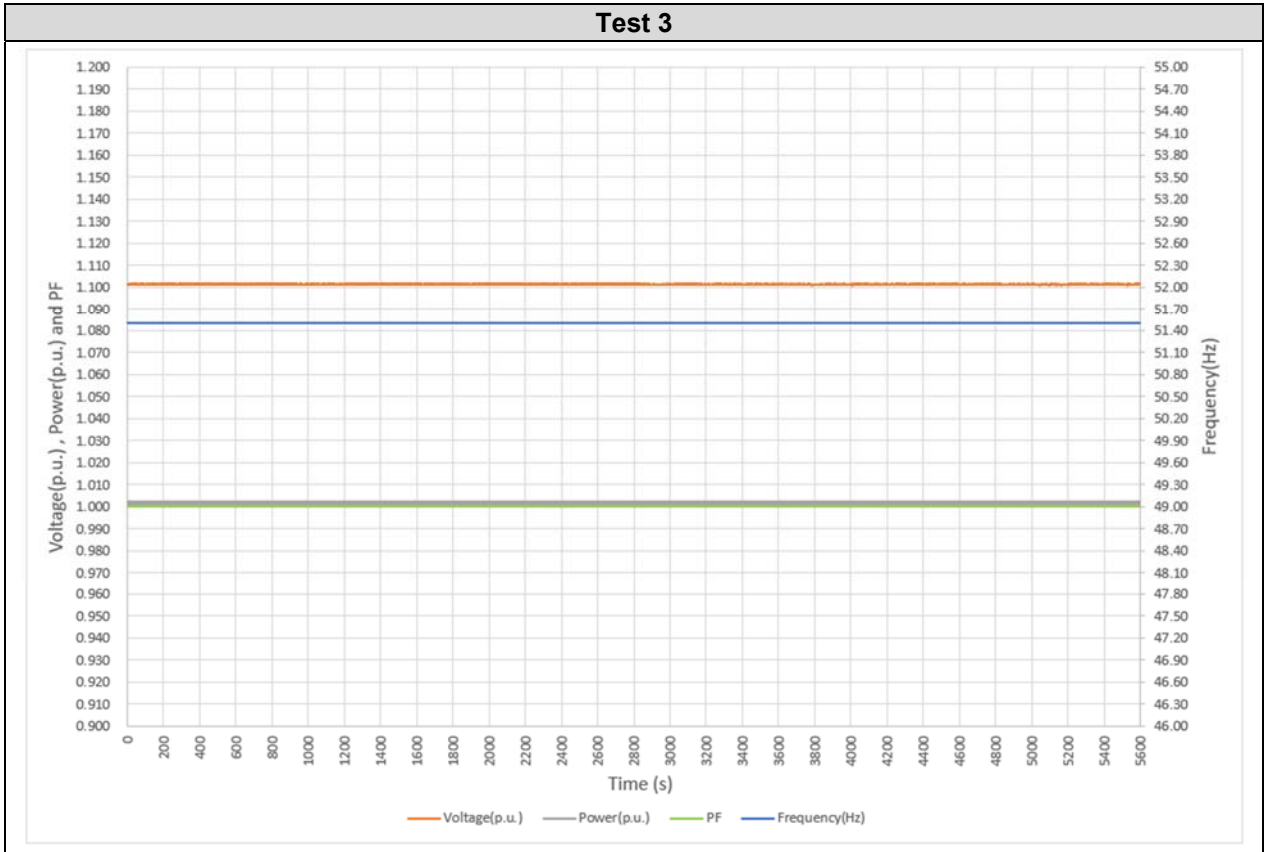
Period of test 15 minutes

Test results are graphically shown in following pages.

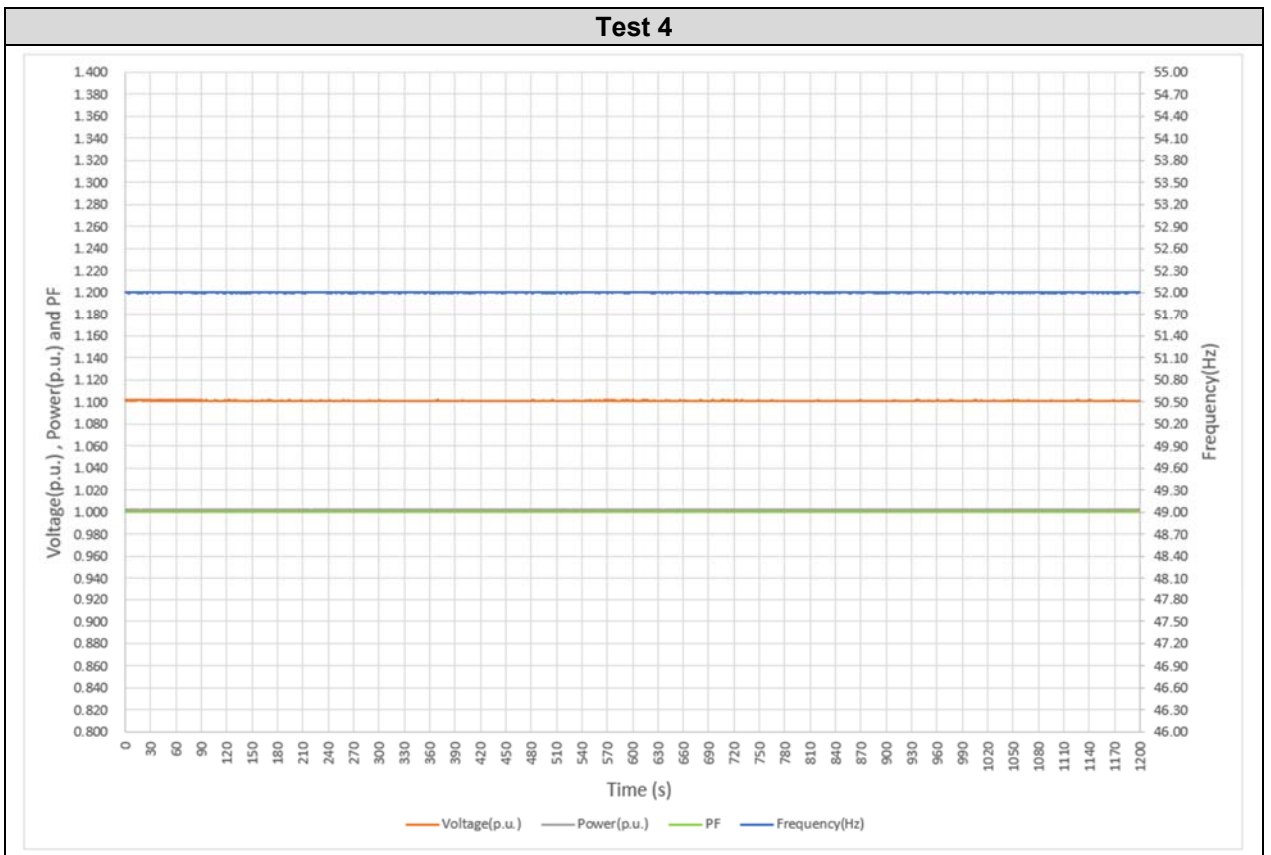




Test 3



Test 4



## 4.2 POWER QUALITY

### 4.2.1 Harmonics

For Power Generating Modules of Registered Capacity of less than 75 A per phase (ie 50 kW) the test requirements are specified in Annex A.7.1.5. These tests should be carried out as specified in BS EN 61000-3-12 The results need to comply with the limits of Table 2 of BS EN 61000-3-12 for single phase equipment and Table 3 of BS EN 61000-3-12 for three phase equipment.

Power Generating Modules with emissions close to the limits laid down in BS EN 61000-3-12 may require the installation of a transformer between 2 and 4 times the rating of the Power Generating Module in order to accept the connection to a Distribution Network.

For Power Generating Modules of Registered Capacity of greater than 145 A per phase (ie 136 kW) the installation must be designed in accordance with EREC G5.

Measures have been repeated at 50%P<sub>n</sub> and 100%P<sub>n</sub>.

Following tables show the test results:

Power Generating Module rating per phase (rpp)		136	kVA		Harmonic % = Measured Value (A) x 23/rating per phase (kVA)	
Phase A						
Harmonic	At 45-55% of <b>Registered Capacity</b>		100% of <b>Registered Capacity</b>		Limit in BS EN 61000-3-12	
	Measured Value MV in Amps	(%)	Measured Value MV in Amps	(%)	1 Phase	3 Phase
2	0.044	0.030	0.096	0.066	8%	8%
3	0.101	0.070	0.082	0.057	21.6%	Not stated
4	0.036	0.025	0.073	0.050	4%	4%
5	0.185	0.127	0.183	0.126	10.7%	10.7%
6	0.040	0.028	0.086	0.059	2.67%	2.67%
7	0.152	0.105	0.111	0.077	7.2%	7.2%
8	0.041	0.028	0.060	0.042	2%	2%
9	0.062	0.043	0.061	0.042	3.8%	Not stated
10	0.037	0.025	0.063	0.044	1.6%	1.6%
11	0.153	0.106	0.245	0.169	3.1%	3.1%
12	0.044	0.030	0.081	0.056	1.33%	1.33%
13	0.055	0.038	0.062	0.043	2%	2%
THD	--	0.281	--	0.365	23%	13%
PWHD	--	0.867	--	1.146	23%	22%

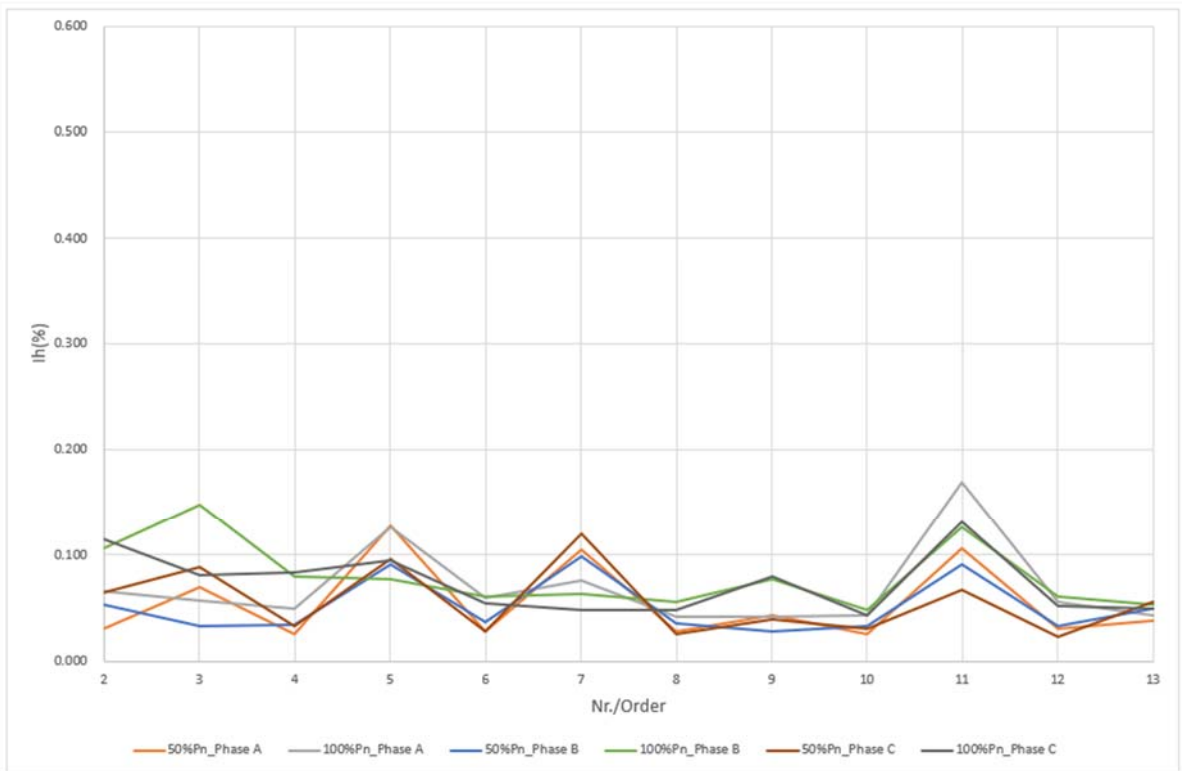
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Phase B						
Harmonic	At 45-55% of <b>Registered Capacity</b>		100% of <b>Registered Capacity</b>		Limit in BS EN 61000-3-12	
	Measured Value MV in Amps	(%)	Measured Value MV in Amps	(%)	1 Phase	3 Phase
2	0.078	0.054	0.153	0.106	8%	8%
3	0.049	0.034	0.215	0.148	21.6%	Not stated
4	0.050	0.034	0.116	0.080	4%	4%
5	0.133	0.092	0.111	0.077	10.7%	10.7%
6	0.053	0.037	0.088	0.061	2.67%	2.67%
7	0.143	0.099	0.092	0.063	7.2%	7.2%
8	0.052	0.036	0.081	0.056	2%	2%
9	0.041	0.028	0.112	0.077	3.8%	Not stated
10	0.048	0.033	0.070	0.048	1.6%	1.6%
11	0.132	0.091	0.183	0.126	3.1%	3.1%
12	0.049	0.034	0.089	0.061	1.33%	1.33%
13	0.073	0.050	0.078	0.054	2%	2%
THD	--	0.278	--	0.389	23%	13%
PWHD	--	0.963	--	1.199	23%	22%

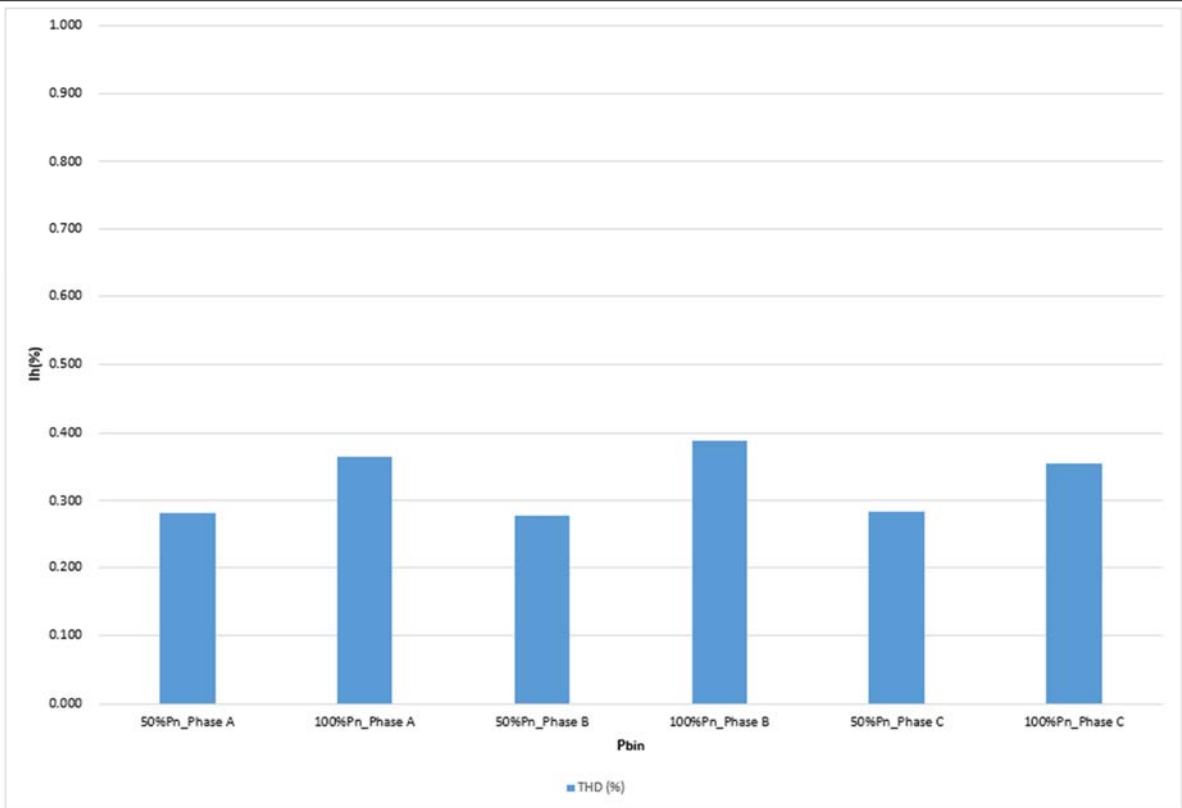
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Phase C						
Harmonic	At 45-55% of <b>Registered Capacity</b>		100% of <b>Registered Capacity</b>		Limit in BS EN 61000-3-12	
	Measured Value MV in Amps	(%)	Measured Value MV in Amps	(%)	1 Phase	3 Phase
2	0.094	0.065	0.167	0.115	8%	8%
3	0.128	0.088	0.118	0.082	21.6%	Not stated
4	0.048	0.033	0.122	0.084	4%	4%
5	0.140	0.097	0.137	0.095	10.7%	10.7%
6	0.041	0.028	0.080	0.055	2.67%	2.67%
7	0.175	0.120	0.070	0.048	7.2%	7.2%
8	0.037	0.025	0.070	0.048	2%	2%
9	0.057	0.040	0.116	0.080	3.8%	Not stated
10	0.045	0.031	0.064	0.044	1.6%	1.6%
11	0.098	0.068	0.191	0.131	3.1%	3.1%
12	0.034	0.024	0.075	0.052	1.33%	1.33%
13	0.082	0.056	0.072	0.050	2%	2%
THD	--	0.285	--	0.354	23%	13%
PWHD	--	0.914	--	1.066	23%	22%

**Current Harmonics**



**THD**



#### 4.2.2 Voltage fluctuations and Flicker

These tests should be undertaken in accordance with EREC G98 Annex A1 A.1.3.3 (Inverter connected) or Annex A2 A.2.3.3 (Synchronous).

The measurements of voltage fluctuations have been measured according to the standard, at 100 % of the nominal power value of the inverter.

The test impedance is recorded in the table below:

Test Impedance	R	0.4	$\Omega$	X	0.25	$\Omega$
Standard Impedance	R	0.4	$\Omega$	X	0.25	$\Omega$
Maximum Impedance	R	0.4	$\Omega$	X	0.25	$\Omega$

Starting operation and Stopping operation			
Pbin (%)	100%		
Phase A			
	Limit	Starting measured values	Stopping measured values
PST	≤ 1	0.058	0.044
PLT	≤ 0.65	0.052	0.052
dc	≤ 3.30%	0.065%	0.115%
d(t)	≤ 3.30%	0.000%	0.000%
dmax	4%	0.209%	0.270%
Phase B			
	Limit	Starting measured values	Stopping measured values
PST	≤ 1	0.043	0.062
PLT	≤ 0.65	0.054	0.054
dc	≤ 3.30%	0.000%	0.221%
d(t)	≤ 3.30%	0.000%	0.000%
dmax	4%	0.000%	0.288%
Phase C			
	Limit	Starting measured values	Stopping measured values
PST	≤ 1	0.087	0.106
PLT	≤ 0.65	0.098	0.098
dc	≤ 3.30%	0.014%	0.193%
d(t)	≤ 3.30%	0.000%	0.000%
dmax	4%	0.149%	0.616%

As it can be seen in the next screenshots, this test has two steps:

1. Starting operation
2. Stopping operation

All values are the most unfavorable of the two steps.

Starting operation and Stopping operation

100% Pn

Phase A

Flicker Mode  
Flicker

Range Over

U1	U2	U3	U4	U5	U6	U7
I1	I2	I3	I4	I5	I6	I7

SCL  Line Filter

AVG  Freq Filter

CH: 1 2 3

4 5 6 7

Count  2/2 Complete

Interval  00:00s/10:00s

Element	1					
Volt Range	1000 V/50Hz	Element1	Judgement	<span style="color: green; font-weight: bold;">Pass</span>		
Un (U1)	541.651V	Total	Judgement	<span style="color: green; font-weight: bold;">Pass</span>		
Freq (U1)	50.000Hz	(Element1,2,3)				
Dmin	0.10%					

	dc[%]	dmax[%]	d(t)[ms]	Pst	Plt
Limit	3.30	4.00	500	1.00	0.65
			3.30%		N:2
No. 1	0.065 <span style="color: green;">Pass</span>	0.115 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.044 <span style="color: green;">Pass</span>	
2	0.209 <span style="color: green;">Pass</span>	0.270 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.058 <span style="color: green;">Pass</span>	
Result	<span style="color: green; font-weight: bold;">Pass</span>	<span style="color: green; font-weight: bold;">Pass</span>	<span style="color: green; font-weight: bold;">Pass</span>	<span style="color: green; font-weight: bold;">Pass</span>	0.052 <span style="color: green; font-weight: bold;">Pass</span>

ΣA(3V3A)

U1 1000 V  
I1 2 V  
Sync Src: U1  
Integral: Reset

U2 1000 V  
I2 2 V  
Sync Src: U1  
Integral: Reset

U3 1000 V  
I3 2 V  
Sync Src: U1  
Integral: Reset

Element 4

U4 1000 V  
I4 2 V  
Sync Src: U1  
Integral: Reset

Element 5

U5 1000 V  
I5 50 A  
Sync Src: U1  
Integral: Reset

Update: 688 Runtime: 5:31:18 144% 10% 2020-12-24 14:06:31

Phase B

Flicker Mode  
Flicker

Range Over

U1	U2	U3	U4	U5	U6	U7
I1	I2	I3	I4	I5	I6	I7

SCL  Line Filter

AVG  Freq Filter

PA\_00001.png

CH: 1 2 3

4 5 6 7

Count  2/2 Complete

Interval  00:00s/10:00s

Element	2					
Volt Range	1000 V/50Hz	Element2	Judgement	<span style="color: green; font-weight: bold;">Pass</span>		
Un (U2)	541.834V	Total	Judgement	<span style="color: green; font-weight: bold;">Pass</span>		
Freq (U2)	50.000Hz	(Element1,2,3)				
Dmin	0.10%					

	dc[%]	dmax[%]	d(t)[ms]	Pst	Plt
Limit	3.30	4.00	500	1.00	0.65
			3.30%		N:2
No. 1	0.000 <span style="color: green;">Pass</span>	0.000 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.043 <span style="color: green;">Pass</span>	
2	0.221 <span style="color: green;">Pass</span>	0.288 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.062 <span style="color: green;">Pass</span>	
Result	<span style="color: green; font-weight: bold;">Pass</span>	<span style="color: green; font-weight: bold;">Pass</span>	<span style="color: green; font-weight: bold;">Pass</span>	<span style="color: green; font-weight: bold;">Pass</span>	0.054 <span style="color: green; font-weight: bold;">Pass</span>

ΣA(3V3A)

U1 1000 V  
I1 2 V  
Sync Src: U1  
Integral: Reset

U2 1000 V  
I2 2 V  
Sync Src: U1  
Integral: Reset

U3 1000 V  
I3 2 V  
Sync Src: U1  
Integral: Reset

Element 4

U4 1000 V  
I4 2 V  
Sync Src: U1  
Integral: Reset

Element 5

U5 1000 V  
I5 50 A  
Sync Src: U1  
Integral: Reset

Update: 691 Runtime: 5:31:23 144% 10% 2020-12-24 14:06:36



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### Phase C

Flicker Mode  
Flicker

Range Over

U1	U2	U3	U4	U5	U6	U7
I1	I2	I3	I4	I5	I6	I7

SCL  Line Filter

AVG  Freq Filter

PA\_00002.png

CH: 1 2 3

4	5	6	7
---	---	---	---

Count 2/2 Complete

Interval 00:00s/10:00s

Element 3

Volt Range 1000 V/50Hz

Un (U3) 541.949V

Freq (U3) 50.000Hz

Dmin 0.10%

Element3 Judgement Pass

Total Judgement Pass

(Element1,2,3)

	dc[%]	dmax[%]	d(t)[ms]	Pst	Plt
Limit	3.30	4.00	500 3.30%	1.00	0.65 N:2
No. 1	0.014 <span style="color: green;">Pass</span>	0.149 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.087 <span style="color: green;">Pass</span>	
2	0.193 <span style="color: green;">Pass</span>	0.616 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.106 <span style="color: green;">Pass</span>	
Result	<span style="color: green;">Pass</span>	<span style="color: green;">Pass</span>	<span style="color: green;">Pass</span>	<span style="color: green;">Pass</span>	0.098 <span style="color: green;">Pass</span>

Σ A[3V3A]

U1 1000 V

I1 2 V

Sync Src: U1

Integral: Reset

Element 2

U2 1000 V

I2 2 V

Sync Src: U1

Integral: Reset

Element 3

U3 1000 V

I3 2 V

Sync Src: U1

Integral: Reset

Element 4

U4 1000 V

I4 2 V

Sync Src: U1

Integral: Reset

Element 5

U5 1000 V

I5 50 A

Sync Src: U1

Integral: Reset

Update: 694

Runtime: 5:31:29

144% 10% x1

2020-12-24 14:06:42

Running operation 2 hours				
Pbin (%)	100%			
	Limit	Phase A	Phase B	Phase C
		Measured values	Measured values	Measured values
PST	≤ 1	0.043	0.045	0.096
PLT	≤ 0.65	0.042	0.047	0.095
dc	≤ 3.30%	0.078%	0.085%	0.050%
d(t)	≤ 3.30%	0.000%	0.000%	0.000%
dmax	4%	0.177%	0.134%	0.147%

As it can be seen in the next screenshots is running operation. The values took of Pst and Plt are the most unfavorable of the twelve steps.

**Running operation**

**100% Pn**

**Phase A**

Flicker Mode: Flicker

Range Over: U1 U2 U3 U4 U5 U6 U7, I1 I2 I3 I4 I5 I6 I7

SCL  Line Filter

AVG  Freq Filter

CH: 1 2 3, 4 5 6 7

Count: 12/12 Complete

Interval: 00:00s/10:00s

Element: 1

Volt Range: 1500 V/50Hz

Un (U1): 540.195V

Freq (U1): 50.000Hz

Dmin: 0.10%

Element1 Judgement: Pass

Total Judgement: Pass (Element1,2,3)

	dc[%]	dmax[%]	d(t)[ms]	Pst	Plt
Limit	3.30	4.00	500 3.30%	1.00	0.65
No. 1	0.006 Pass	0.112 Pass	0.0 Pass	0.043 Pass	
2	0.050 Pass	0.117 Pass	0.0 Pass	0.042 Pass	
3	0.068 Pass	0.114 Pass	0.0 Pass	0.042 Pass	
4	0.059 Pass	0.106 Pass	0.0 Pass	0.041 Pass	
5	0.000 Pass	0.000 Pass	0.0 Pass	0.042 Pass	
6	0.000 Pass	0.000 Pass	0.0 Pass	0.041 Pass	
7	0.060 Pass	0.144 Pass	0.0 Pass	0.043 Pass	
8	0.034 Pass	0.103 Pass	0.0 Pass	0.043 Pass	
9	0.063 Pass	0.177 Pass	0.0 Pass	0.043 Pass	
10	0.078 Pass	0.106 Pass	0.0 Pass	0.043 Pass	
11	0.000 Pass	0.000 Pass	0.0 Pass	0.043 Pass	
12	0.071 Pass	0.115 Pass	0.0 Pass	0.042 Pass	
Result	Pass	Pass	Pass	Pass	0.042 Pass

ΣA(3V3A)

U1 1500 V

I1 2 V

Sync Src: U1

Integral: Reset

U2 1500 V

I2 2 V

Sync Src: U1

Integral: Reset

U3 1500 V

I3 2 V

Sync Src: U1

Integral: Reset

Element 4

U4 1500 V

I4 1 V

Sync Src: U1

Integral: Reset

Element 5

U5 1500 V

I5 2 V

Sync Src: U1

Integral: Reset

Update: 3816

Runtime: 5:11:15

137% 18% 2021-02-02 13:18:36

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Phase B

Flicker Mode  
Flicker

Range Over

U1	U2	U3	U4	U5	U6	U7
I1	I2	I3	I4	I5	I6	I7

SCL  Line Filter

AVG  Freq Filter

PA\_00000.png

CH: 1 2 3  
4 5 6 7

Count 12/12 Complete

Interval 00:00s/10:00s

Element 2

Volt Range 1500 V/50Hz

Un (U2) 540.148V

Freq (U2) 50.000Hz

Dmin 0.10%

	dc[%]	dmax[%]	d(t)[ms]	Pst	Pit
Limit	3.30	4.00	500 3.30%	1.00	0.65 N:12
No. 1	0.010 <span style="color: green;">Pass</span>	0.101 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.047 <span style="color: green;">Pass</span>	
2	0.000 <span style="color: green;">Pass</span>	0.000 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.046 <span style="color: green;">Pass</span>	
3	0.085 <span style="color: green;">Pass</span>	0.121 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.045 <span style="color: green;">Pass</span>	
4	0.000 <span style="color: green;">Pass</span>	0.000 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.045 <span style="color: green;">Pass</span>	
5	0.022 <span style="color: green;">Pass</span>	0.103 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.045 <span style="color: green;">Pass</span>	
6	0.000 <span style="color: green;">Pass</span>	0.000 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.044 <span style="color: green;">Pass</span>	
7	0.072 <span style="color: green;">Pass</span>	0.108 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.044 <span style="color: green;">Pass</span>	
8	0.070 <span style="color: green;">Pass</span>	0.127 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.044 <span style="color: green;">Pass</span>	
9	0.000 <span style="color: green;">Pass</span>	0.000 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.044 <span style="color: green;">Pass</span>	
10	0.000 <span style="color: green;">Pass</span>	0.000 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.044 <span style="color: green;">Pass</span>	
11	0.066 <span style="color: green;">Pass</span>	0.134 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.044 <span style="color: green;">Pass</span>	
12	0.064 <span style="color: green;">Pass</span>	0.113 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.044 <span style="color: green;">Pass</span>	
Result	<span style="color: green;">Pass</span>	<span style="color: green;">Pass</span>	<span style="color: green;">Pass</span>	<span style="color: green;">Pass</span>	0.045 <span style="color: green;">Pass</span>

Update: 3820

Runtime: 5:11:23

37%  
18%

2021-02-02  
13:18:44

ΣA[3V3A]

U1 1500 V  
I1 2 V  
Sync Src: U1  
Integral: Reset

U2 1500 V  
I2 2 V  
Sync Src: U1  
Integral: Reset

U3 1500 V  
I3 2 V  
Sync Src: U1  
Integral: Reset

Element 4

U4 1500 V  
I4 1 V  
Sync Src: U1  
Integral: Reset

Element 5

U5 1500 V  
I5 2 V  
Sync Src: U1  
Integral: Reset

Phase C

Flicker Mode  
Flicker

Range Over

U1	U2	U3	U4	U5	U6	U7
I1	I2	I3	I4	I5	I6	I7

SCL  Line Filter

AVG  Freq Filter

PA\_00001.png

CH: 1 2 3  
4 5 6 7

Count 12/12 Complete

Interval 00:00s/10:00s

Element 3

Volt Range 1500 V/50Hz

Un (U3) 540.432V

Freq (U3) 50.000Hz

Dmin 0.10%

	dc[%]	dmax[%]	d(t)[ms]	Pst	Pit
Limit	3.30	4.00	500 3.30%	1.00	0.65 N:12
No. 1	0.046 <span style="color: green;">Pass</span>	0.114 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.096 <span style="color: green;">Pass</span>	
2	0.037 <span style="color: green;">Pass</span>	0.107 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.095 <span style="color: green;">Pass</span>	
3	0.033 <span style="color: green;">Pass</span>	0.147 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.095 <span style="color: green;">Pass</span>	
4	0.050 <span style="color: green;">Pass</span>	0.116 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.095 <span style="color: green;">Pass</span>	
5	0.050 <span style="color: green;">Pass</span>	0.110 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.095 <span style="color: green;">Pass</span>	
6	0.042 <span style="color: green;">Pass</span>	0.109 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.094 <span style="color: green;">Pass</span>	
7	0.044 <span style="color: green;">Pass</span>	0.129 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.094 <span style="color: green;">Pass</span>	
8	0.046 <span style="color: green;">Pass</span>	0.121 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.094 <span style="color: green;">Pass</span>	
9	0.041 <span style="color: green;">Pass</span>	0.112 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.095 <span style="color: green;">Pass</span>	
10	0.048 <span style="color: green;">Pass</span>	0.116 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.095 <span style="color: green;">Pass</span>	
11	0.039 <span style="color: green;">Pass</span>	0.124 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.094 <span style="color: green;">Pass</span>	
12	0.045 <span style="color: green;">Pass</span>	0.115 <span style="color: green;">Pass</span>	0.0 <span style="color: green;">Pass</span>	0.094 <span style="color: green;">Pass</span>	
Result	<span style="color: green;">Pass</span>	<span style="color: green;">Pass</span>	<span style="color: green;">Pass</span>	<span style="color: green;">Pass</span>	0.095 <span style="color: green;">Pass</span>

Update: 3824

Runtime: 5:11:31

38%  
18%

2021-02-02  
13:18:52

ΣA[3V3A]

U1 1500 V  
I1 2 V  
Sync Src: U1  
Integral: Reset

U2 1500 V  
I2 2 V  
Sync Src: U1  
Integral: Reset

U3 1500 V  
I3 2 V  
Sync Src: U1  
Integral: Reset

Element 4

U4 1500 V  
I4 1 V  
Sync Src: U1  
Integral: Reset

Element 5

U5 1500 V  
I5 2 V  
Sync Src: U1  
Integral: Reset

### 4.2.3 DC Injection

The tests should be carried out on a single Generating Unit. Tests are to be carried out at three defined power levels  $\pm 5\%$ . At 540 V a 136kW three-phase inverter has output current of 145A per phase, so DC limit is 363mA. These tests should be undertaken in accordance with Annex A.7.1.4.4.

Following tables show the test results:

DC injection			
Phase A			
Test power level	10%	55%	100%
Recorded value in Amps	0.017	0.016	0.021
as % of rated AC current	0.01%	0.01%	0.01%
Limit	0.25%	0.25%	0.25%

Phase B			
Test power level	10%	55%	100%
Recorded value in Amps	0.026	0.024	0.029
as % of rated AC current	0.02%	0.02%	0.02%
Limit	0.25%	0.25%	0.25%

Phase C			
Test power level	10%	55%	100%
Recorded value in Amps	0.017	0.013	0.021
as % of rated AC current	0.01%	0.01%	0.01%
Limit	0.25%	0.25%	0.25%

DC injection test result



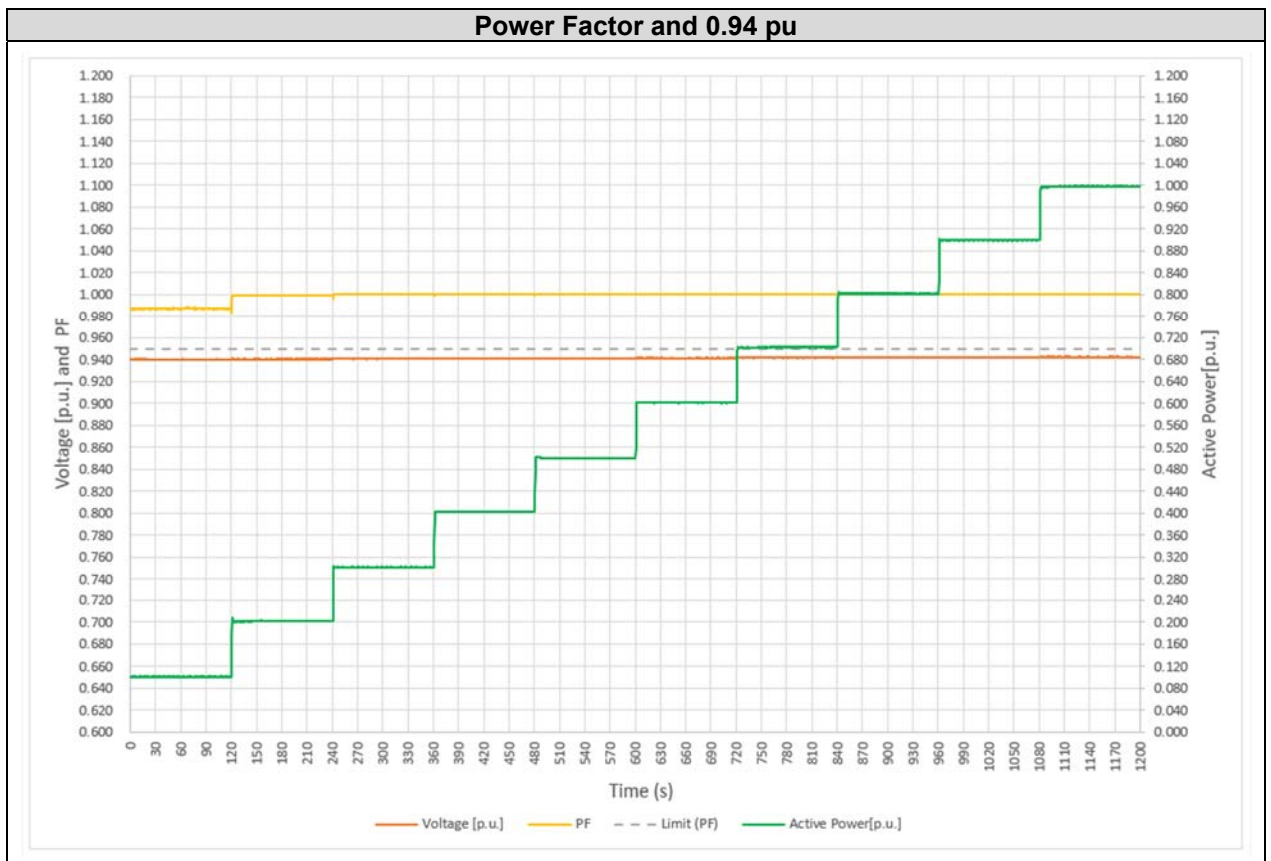
#### 4.2.4 Power Factor

The tests should be carried out on a single Power Generating Module. Tests are to be carried out at three voltage levels and at Registered Capacity. Voltage to be maintained within  $\pm 1.5\%$  of the stated level during the test. These tests should be undertaken in accordance with Annex A.7.1.4.2.

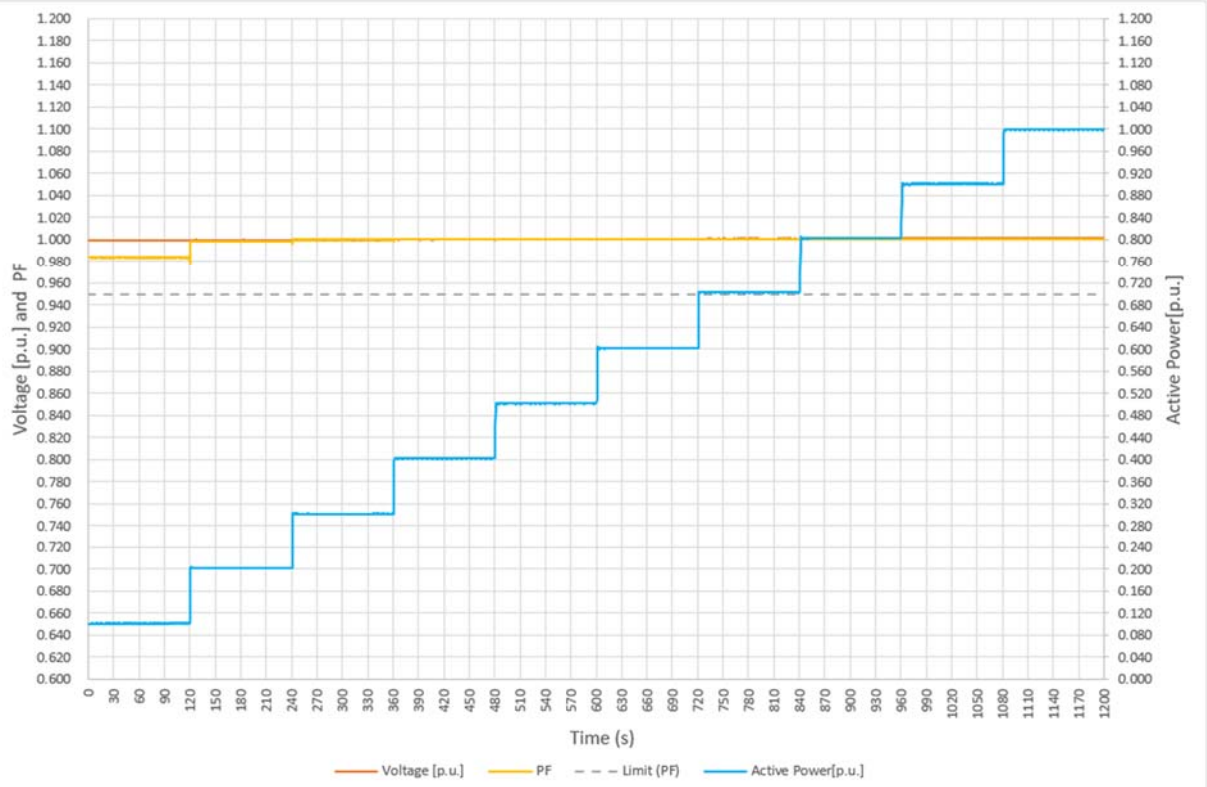
The following table shows the test results at required voltage levels:

Volatge	0.94 pu (508V)	1.00 pu (540V)	1.10 pu (594V)
Measured Volatge value (V)	216.9	230.4	594.6
Measured Power Factor value ( $\cos \varphi$ )	1.00	1.00	1.00
Power Factor Limit	>0.95	>0.95	>0.95

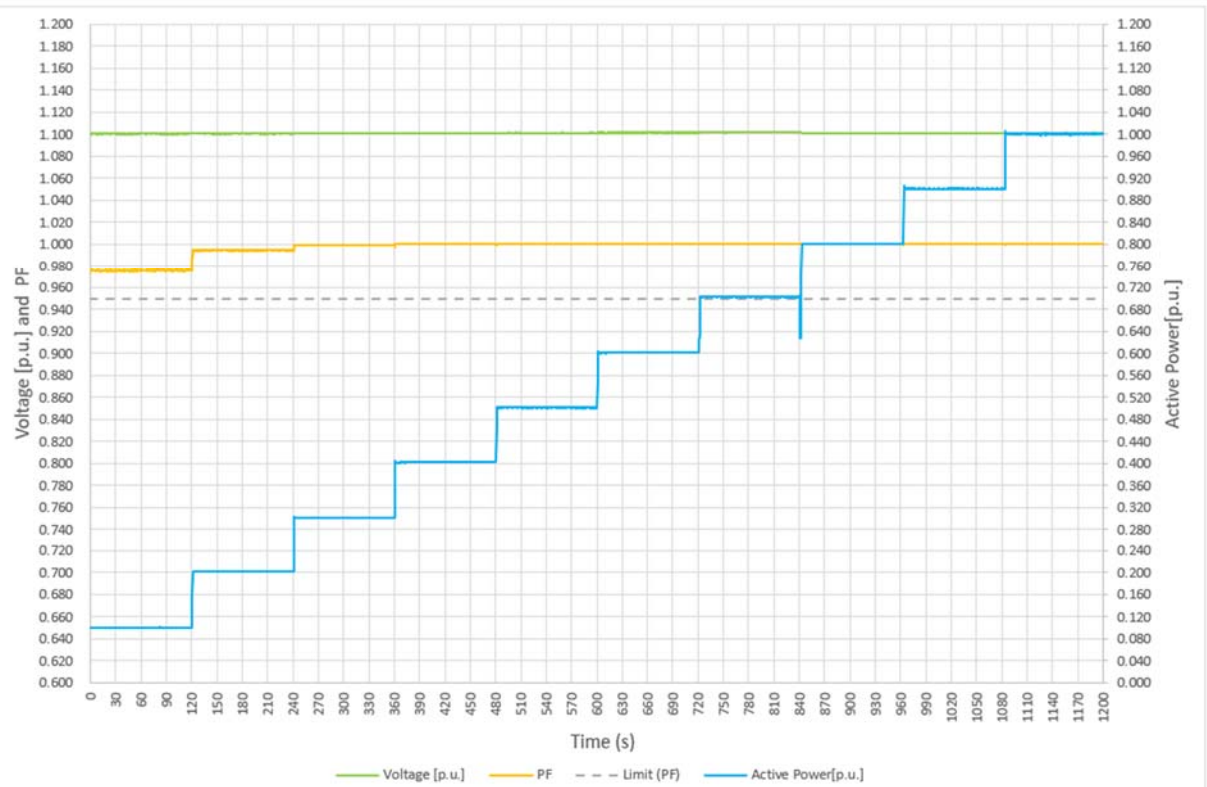
Test results are graphically shown below.



**Power Factor and 1.00pu**



**Power Factor and 1.10pu**



### 4.3 PROTECTION

#### 4.3.1 Frequency tests

These tests should be carried out in accordance with Annex A.7.1.2.3.

To establish a trip frequency, the test frequency should be applied in a slow ramp rate of less than 0.1 Hz/s, or if this is not possible in steps of 0.05 Hz for a duration that is longer than the trip time delay.

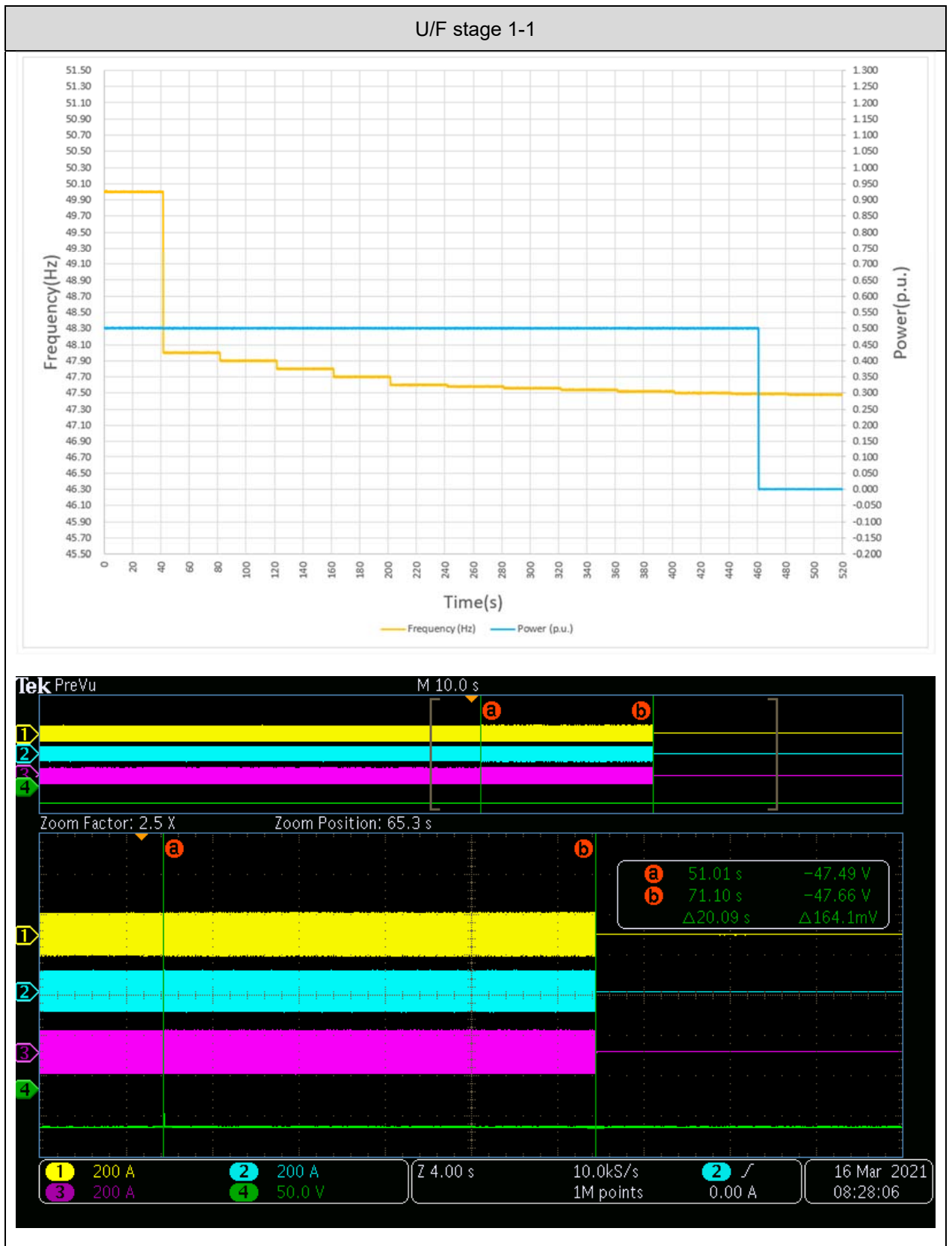
To establish the trip time, the test frequency should be applied starting from 0.3 Hz below or above the recorded trip frequency and should be changed to 0.3 Hz above or below the recorded trip frequency in a single step. For each trip setting five tests shall be carried out.

Following tables show the test results:

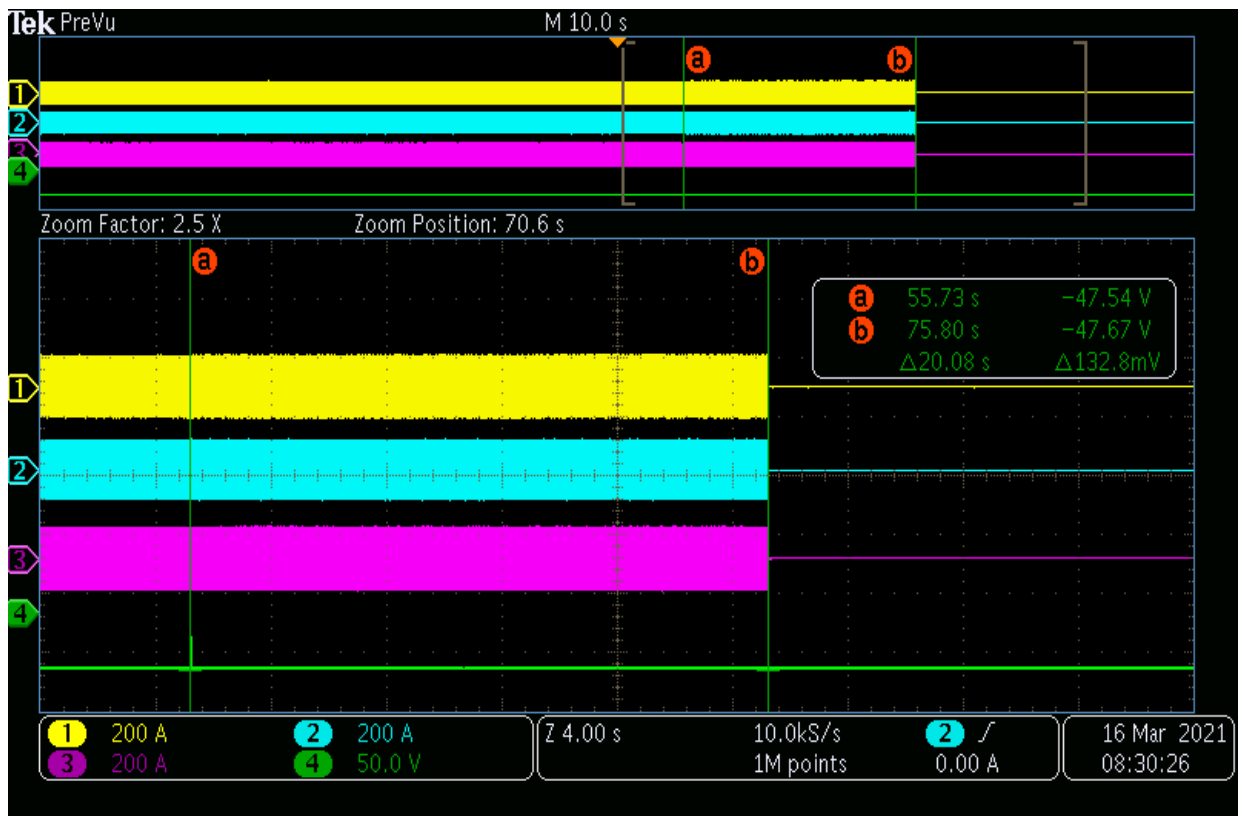
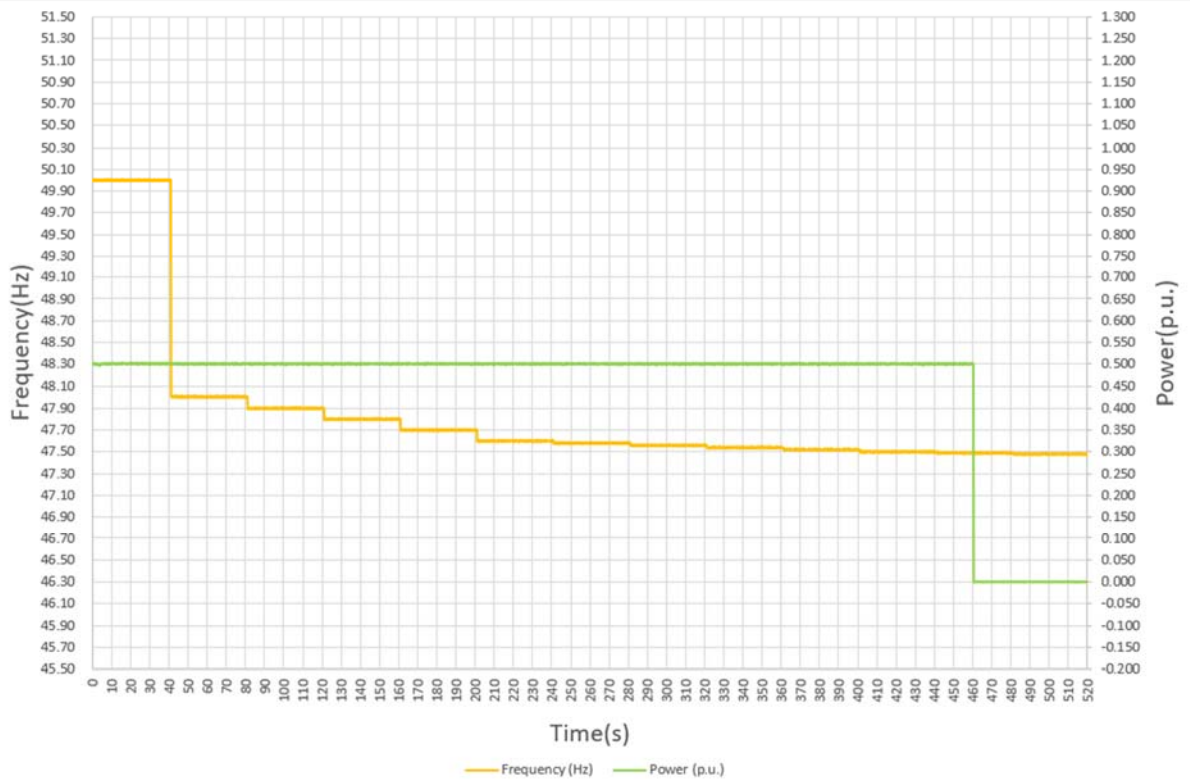
Function	Setting		Trip test (5 times)		"No trip tests"	
	Frequency	Time delay	Frequency (Hz)	Time delay (s)	Frequency /time	Confirm no trip
U/F stage 1	47.5 Hz	20 s	47.5	20.090	47.7 Hz / 25 s	Pass
			47.5	20.080		
			47.5	20.070		
			47.5	20.070		
			47.5	20.060		
U/F stage 2	47 Hz	0.5 s	47.0	0.530	47.2 Hz / 19.98 s	Pass
			47.0	0.528		
			47.0	0.540		
			47.0	0.528		
			47.0	0.538		
					46.8 Hz / 0.48 s	Pass
O/F stage 1	52 Hz	0.5 s	52.0	0.533	51.8 Hz / 89.98 s	Pass
			52.0	0.533		
			52.0	0.522		
			52.0	0.537		
			52.0	0.537		
					52.2 Hz / 0.48 s	Pass



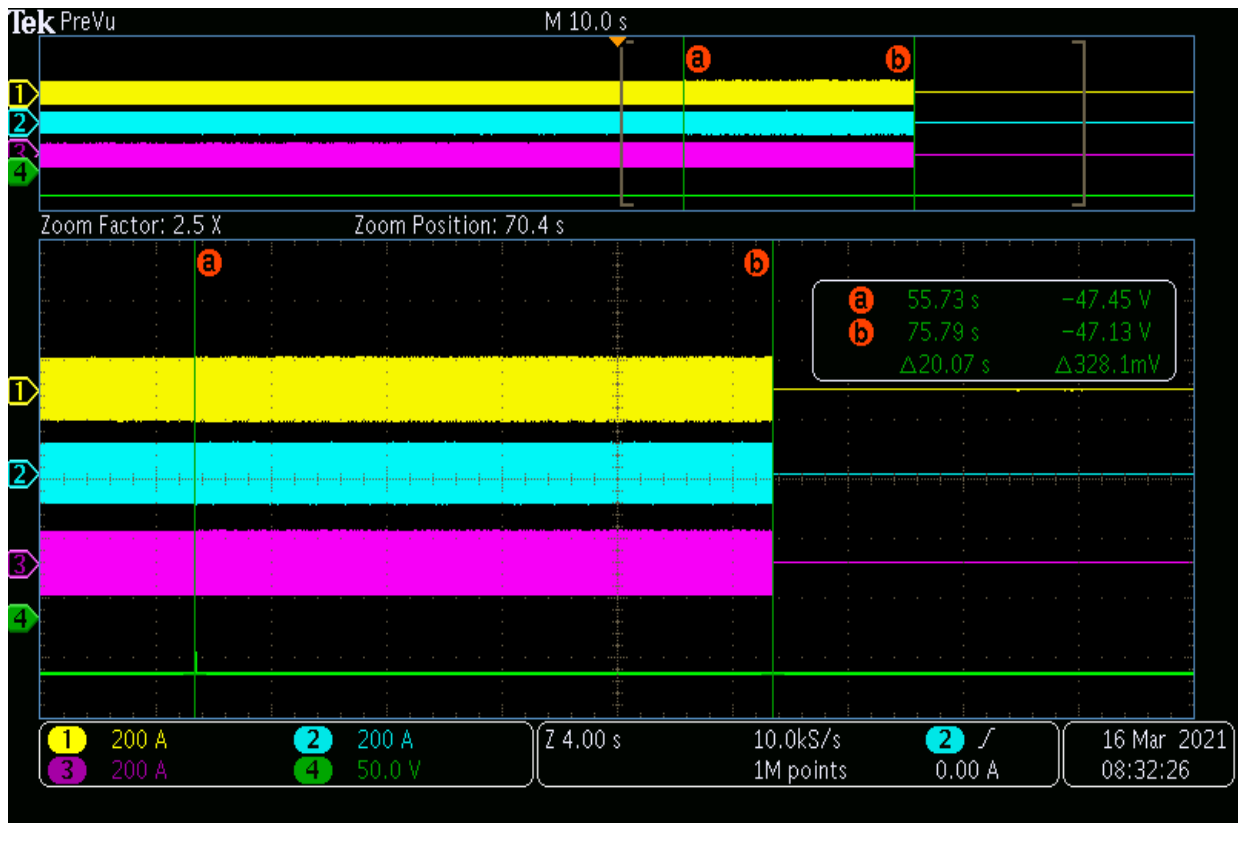
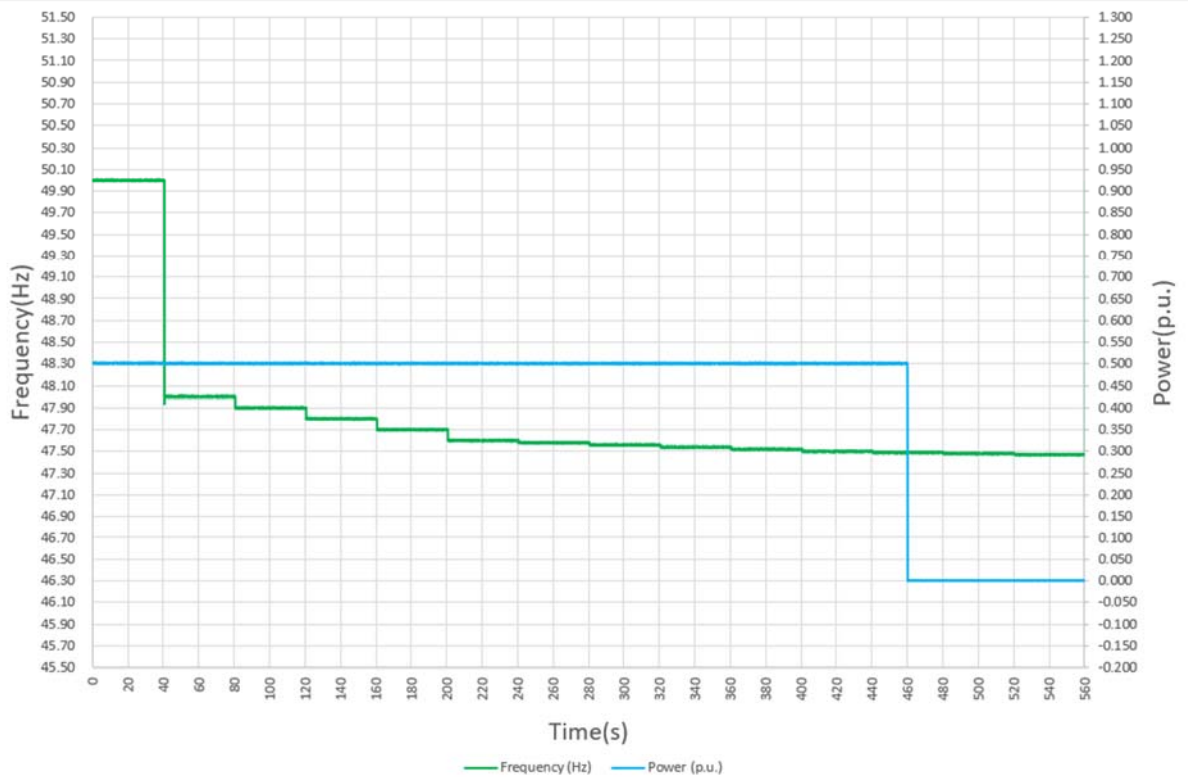
Test results are graphically shown below.



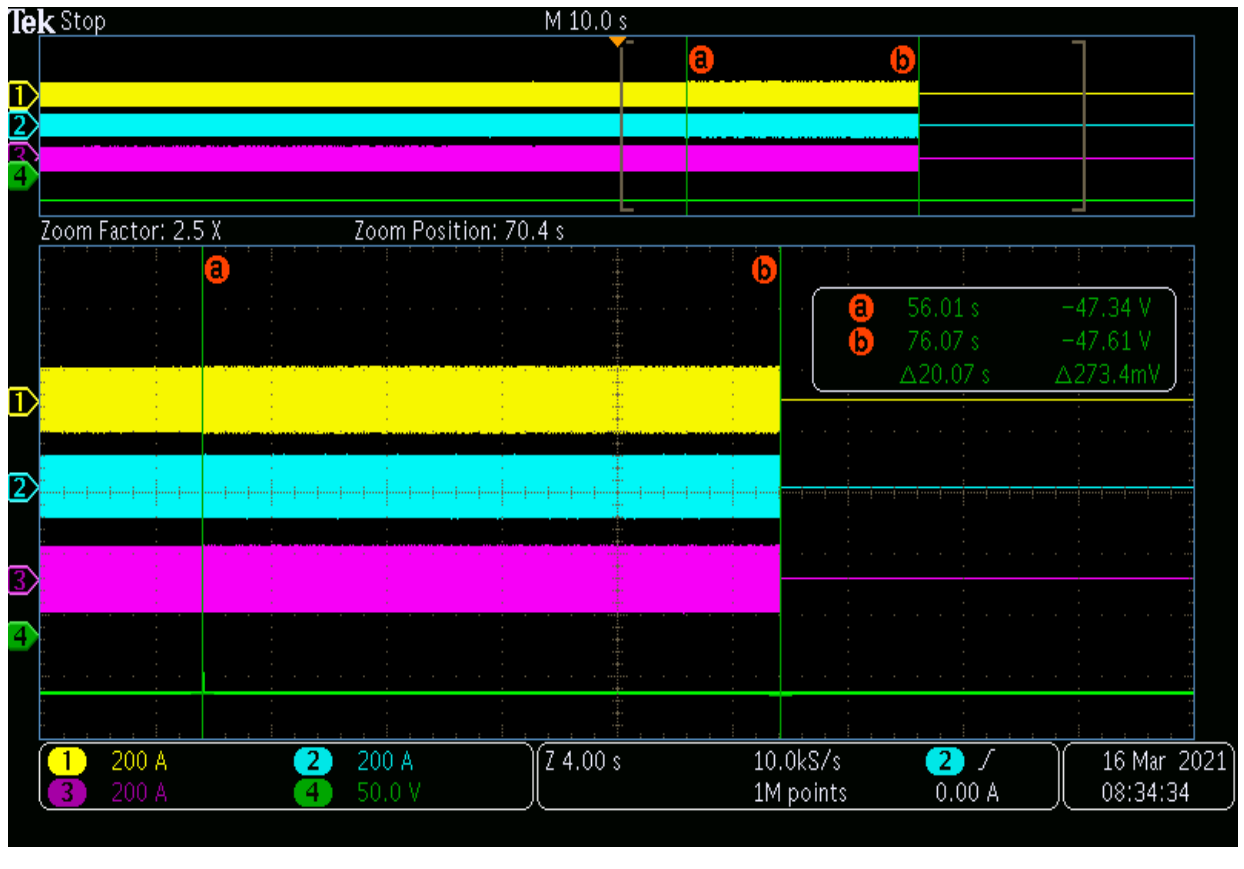
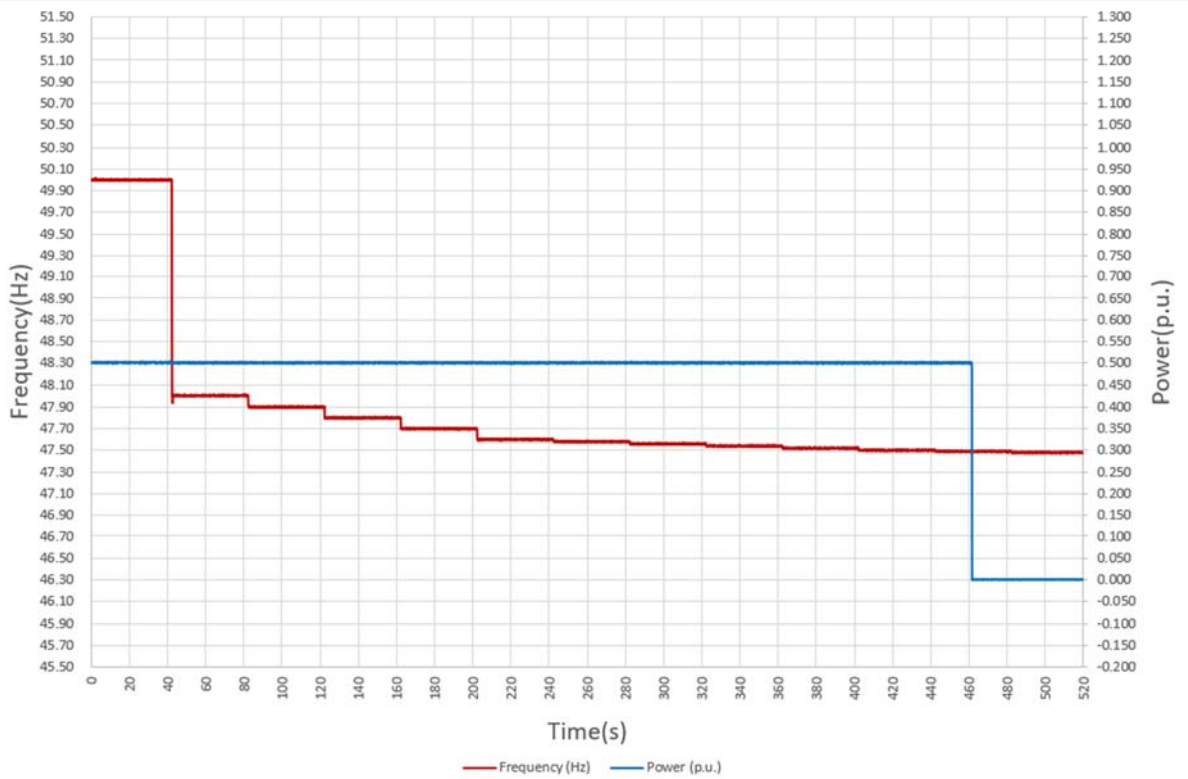
U/F stage 1-2



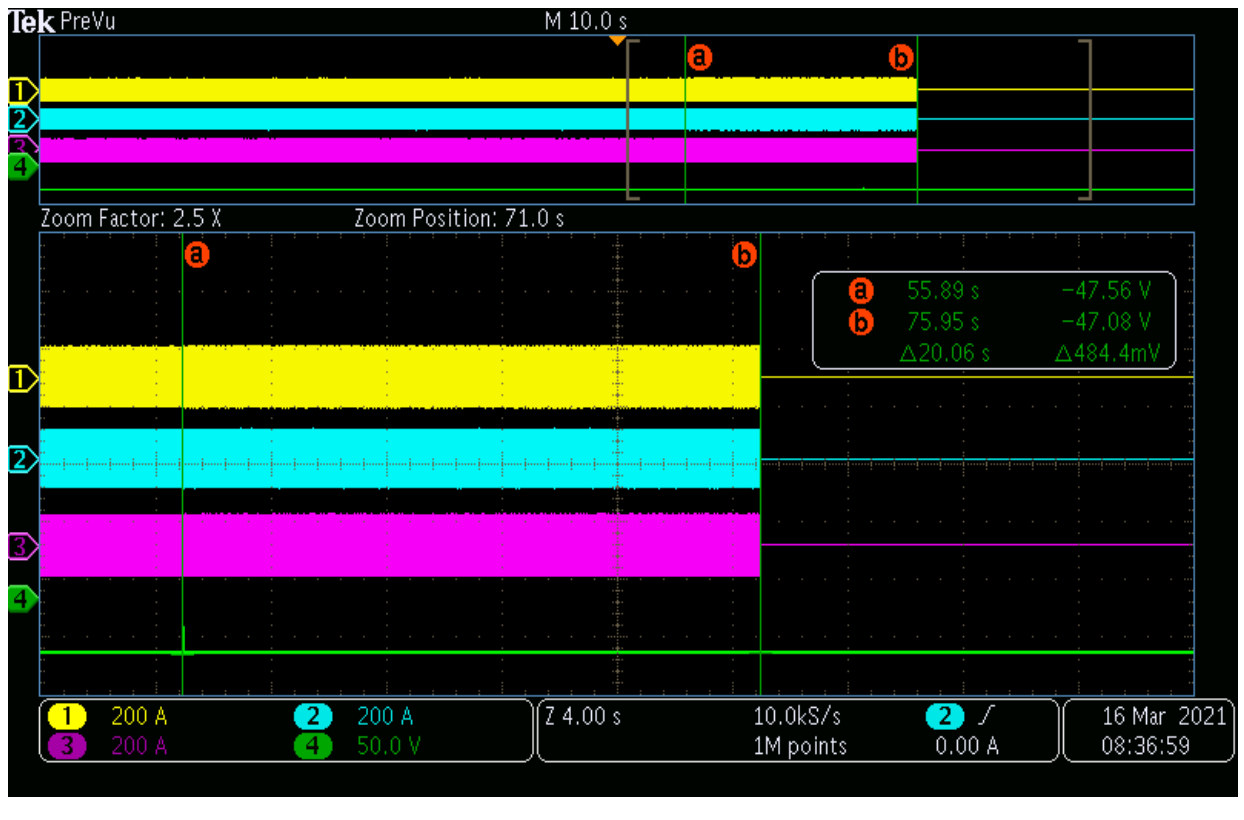
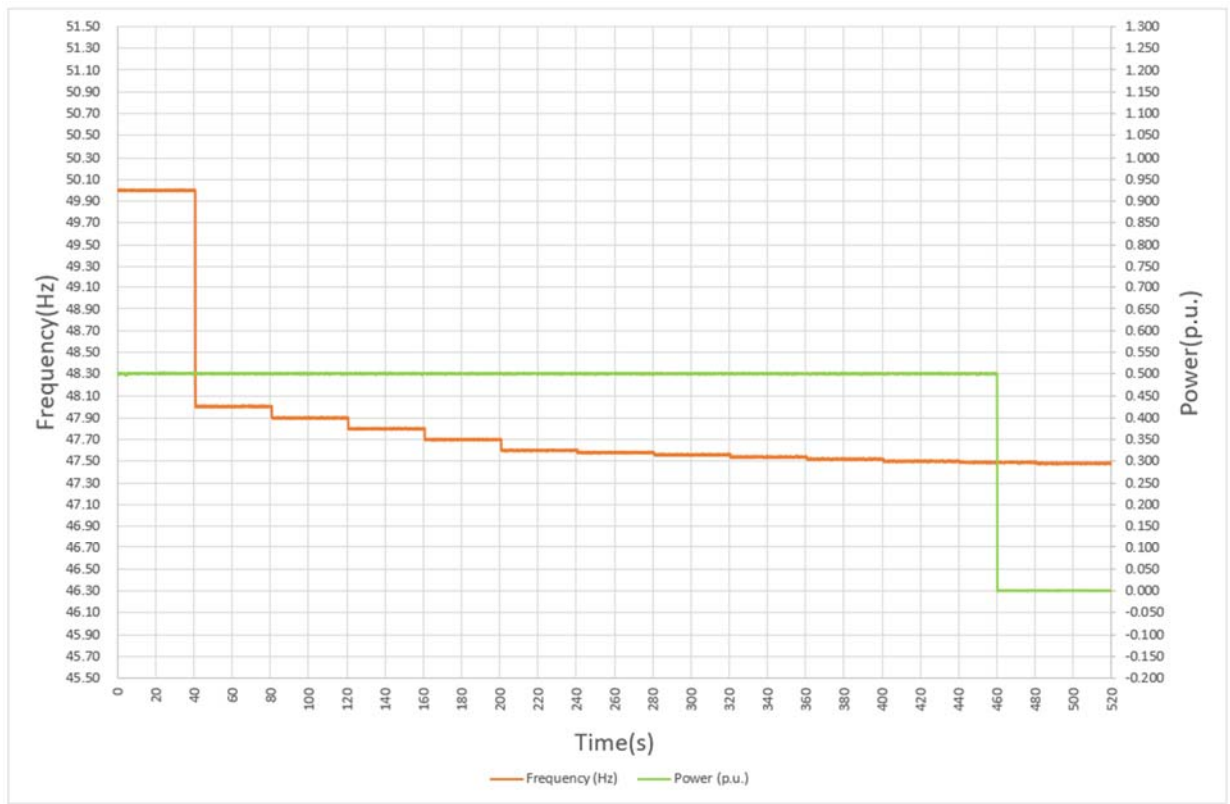
U/F stage 1-3



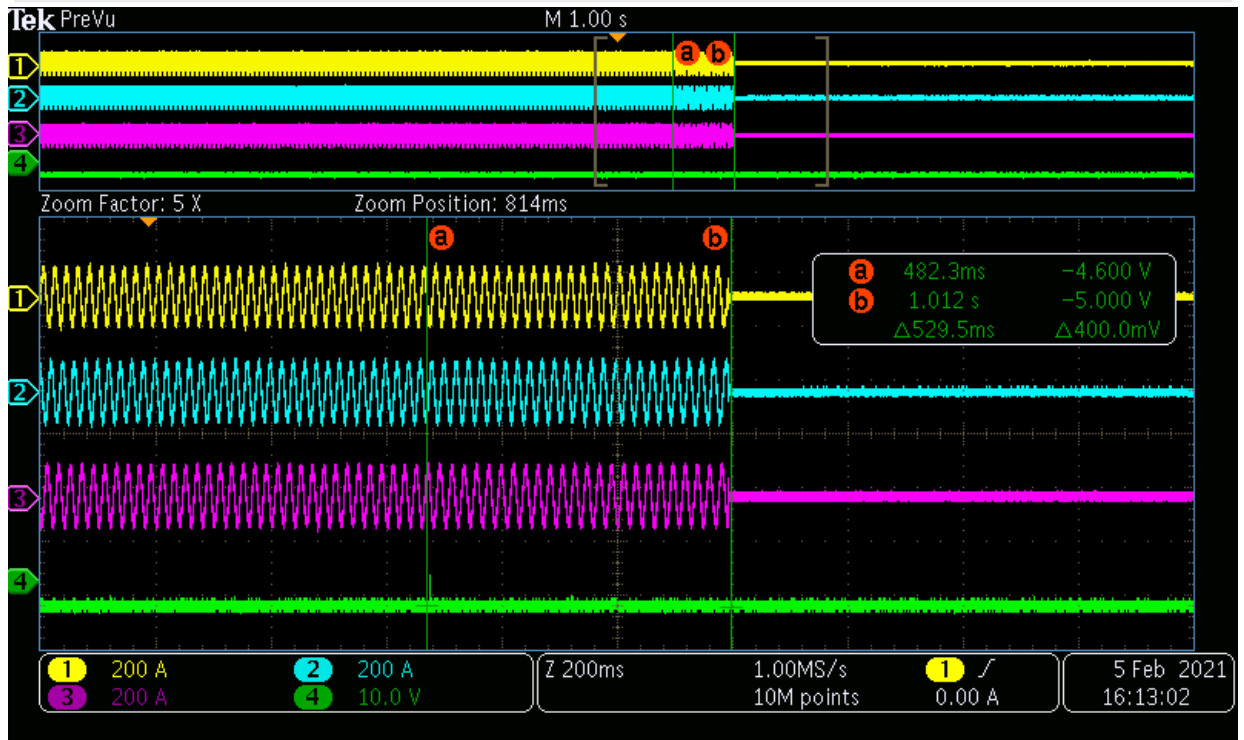
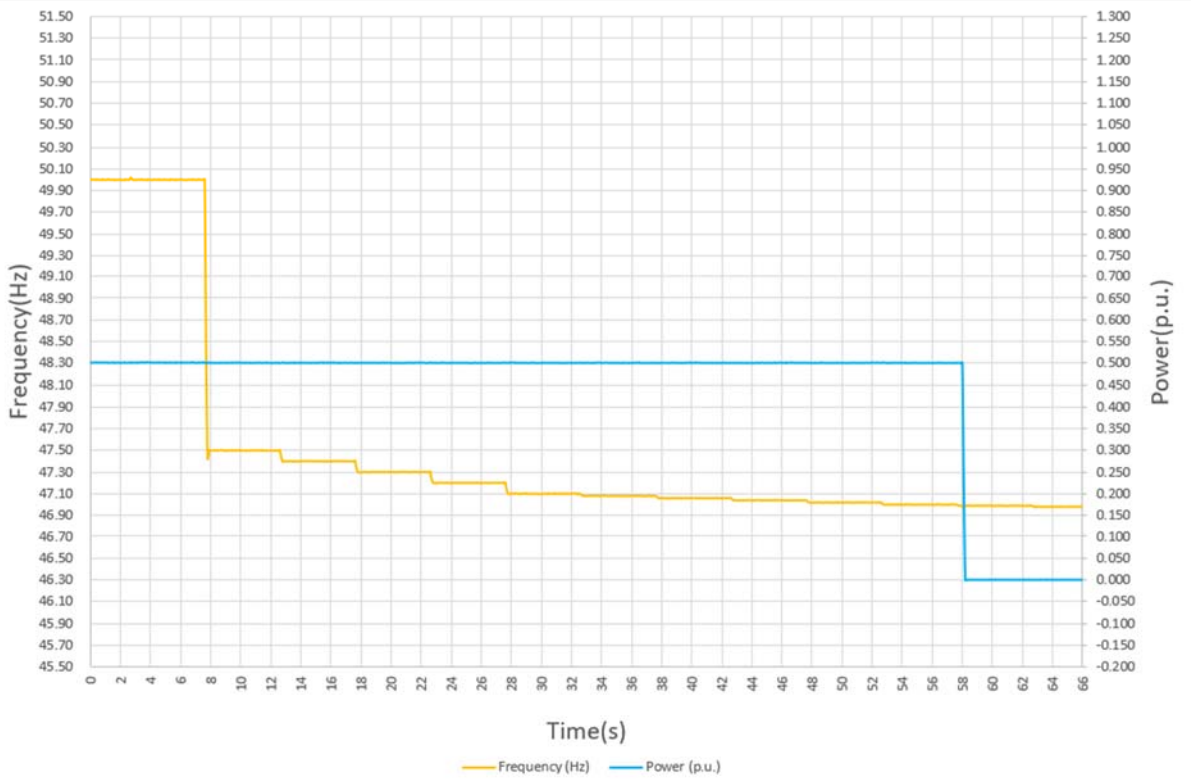
U/F stage 1-4



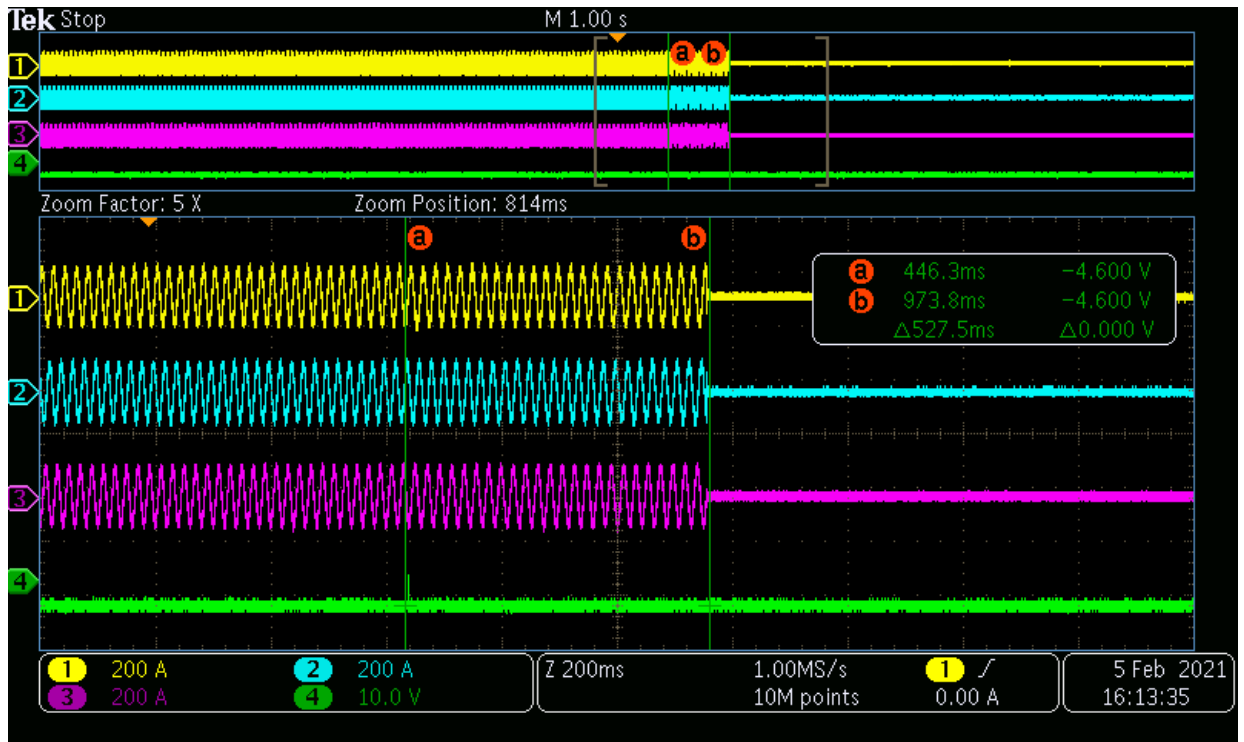
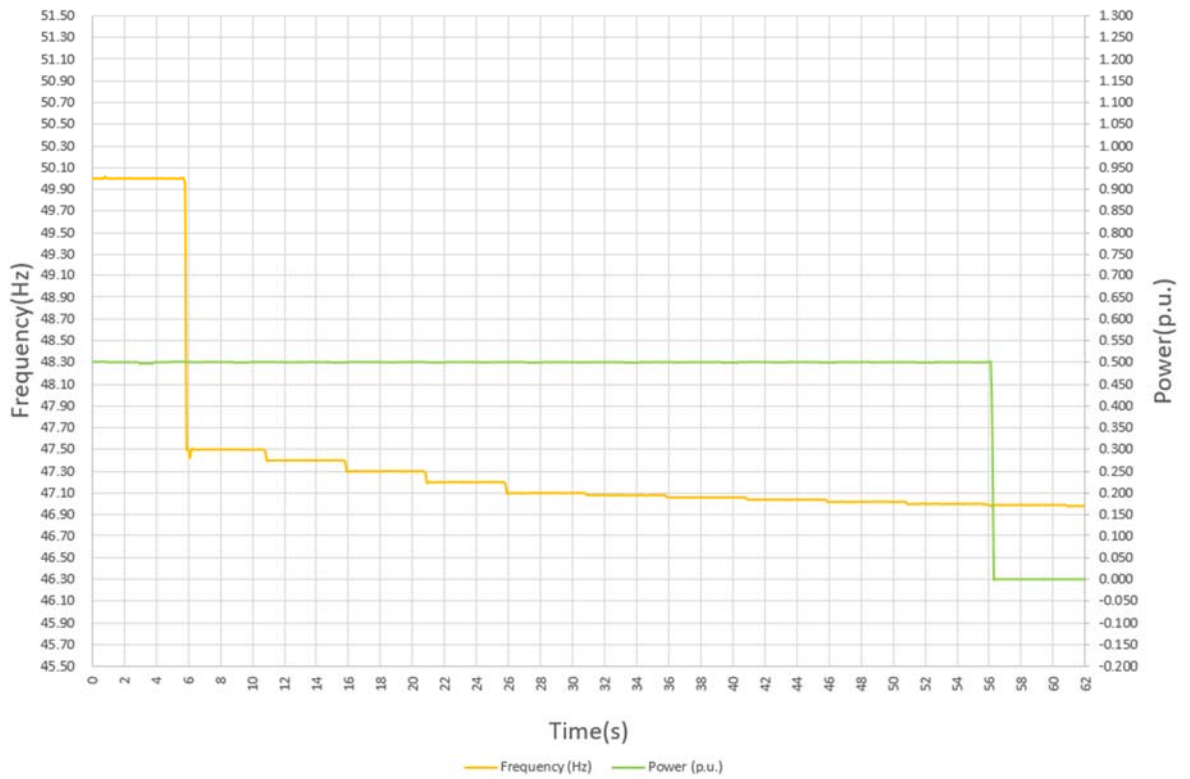
U/F stage 1-5



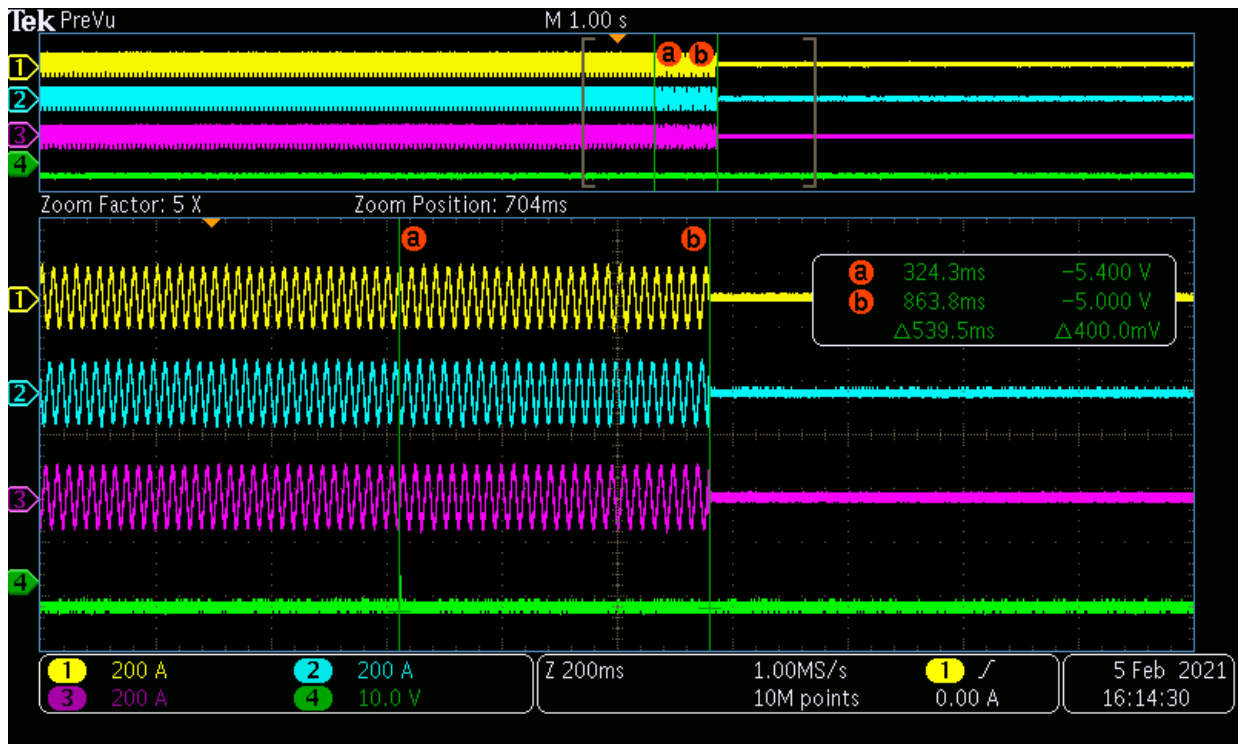
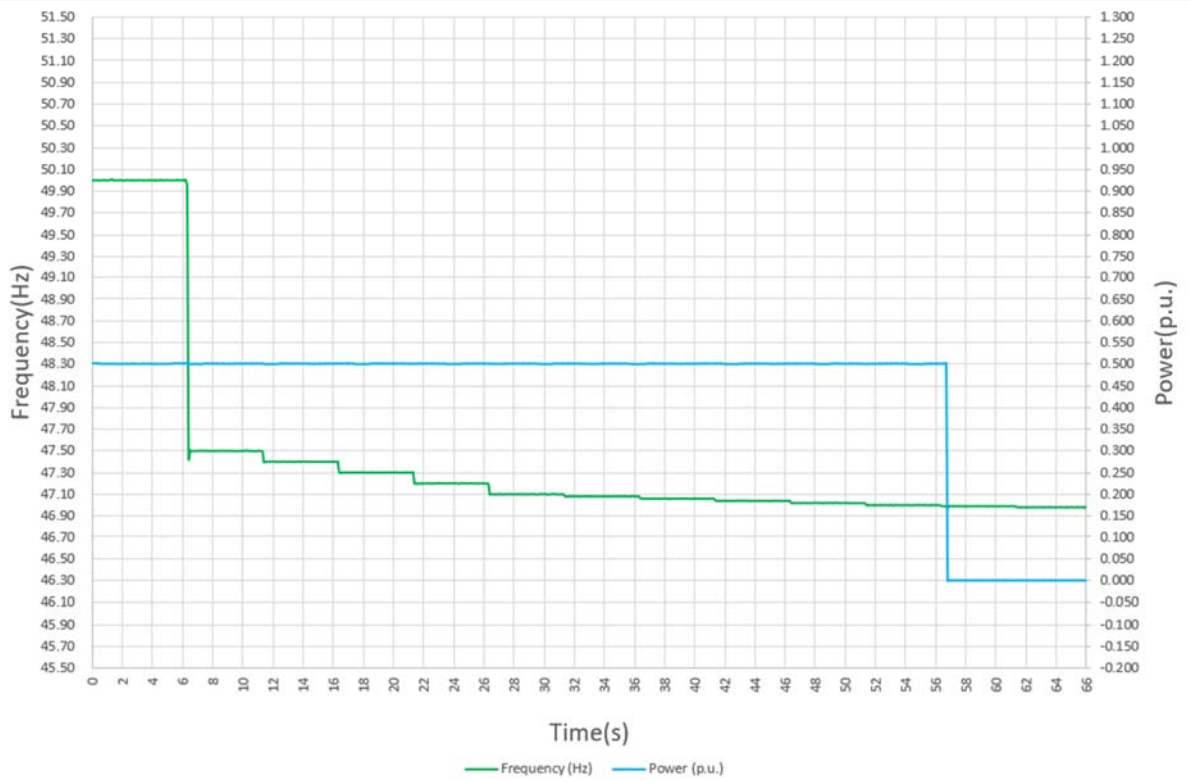
U/F stage 2-1



U/F stage 2-2

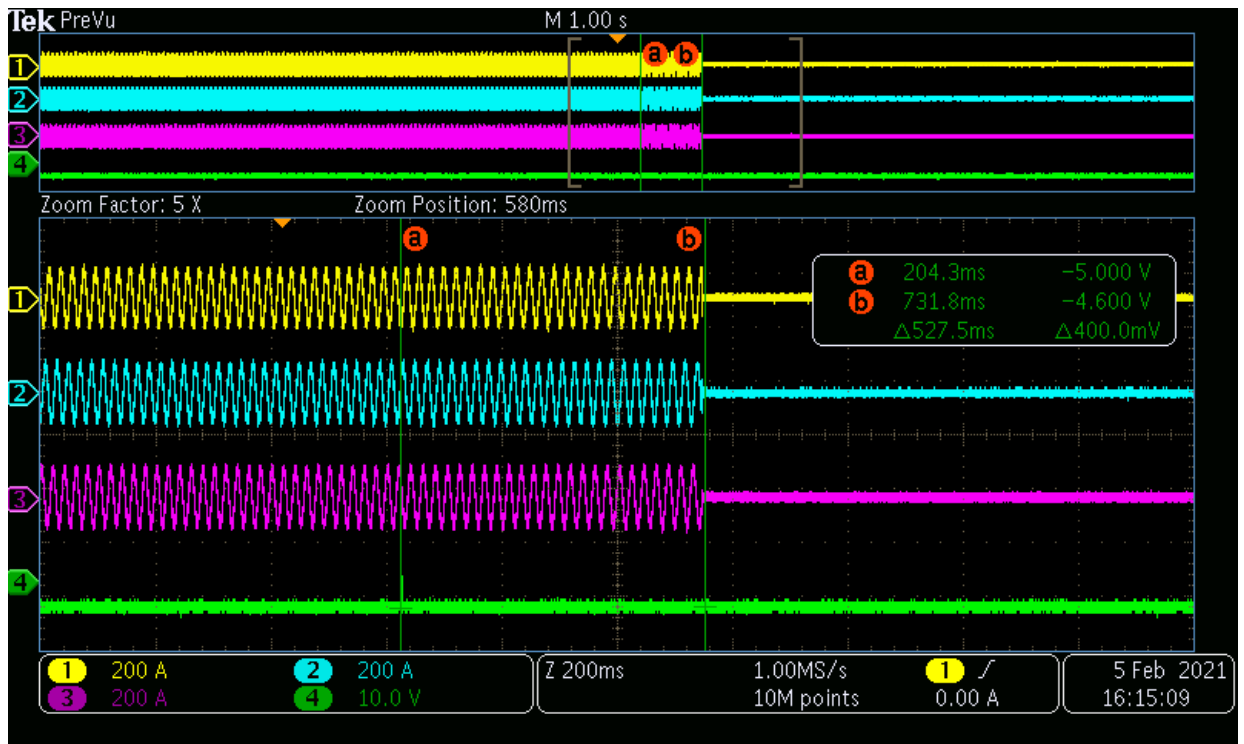
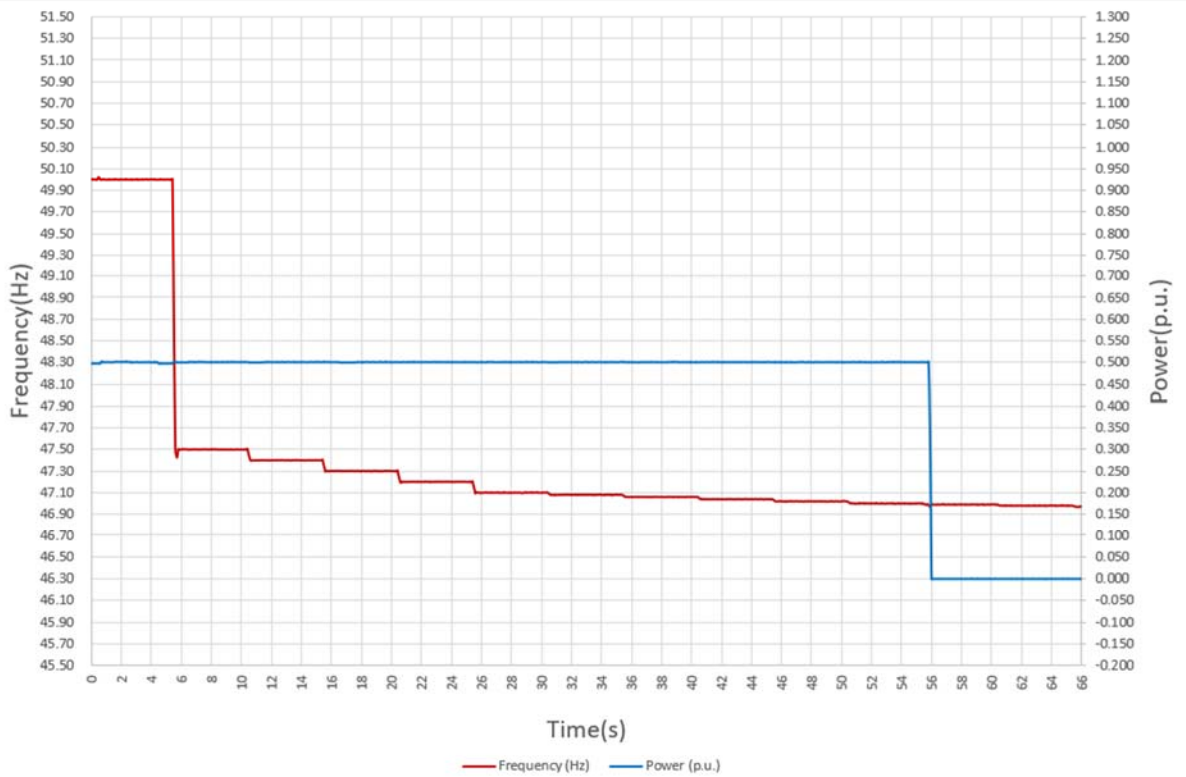


U/F stage 2-3

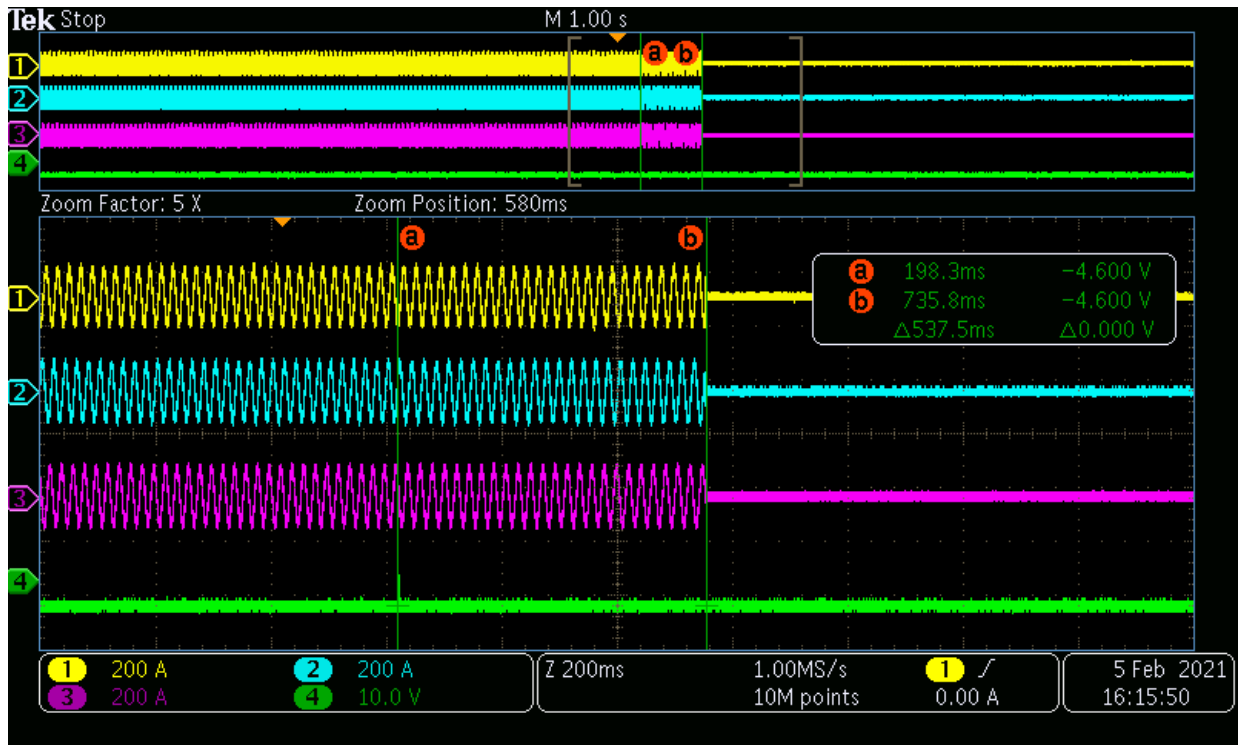
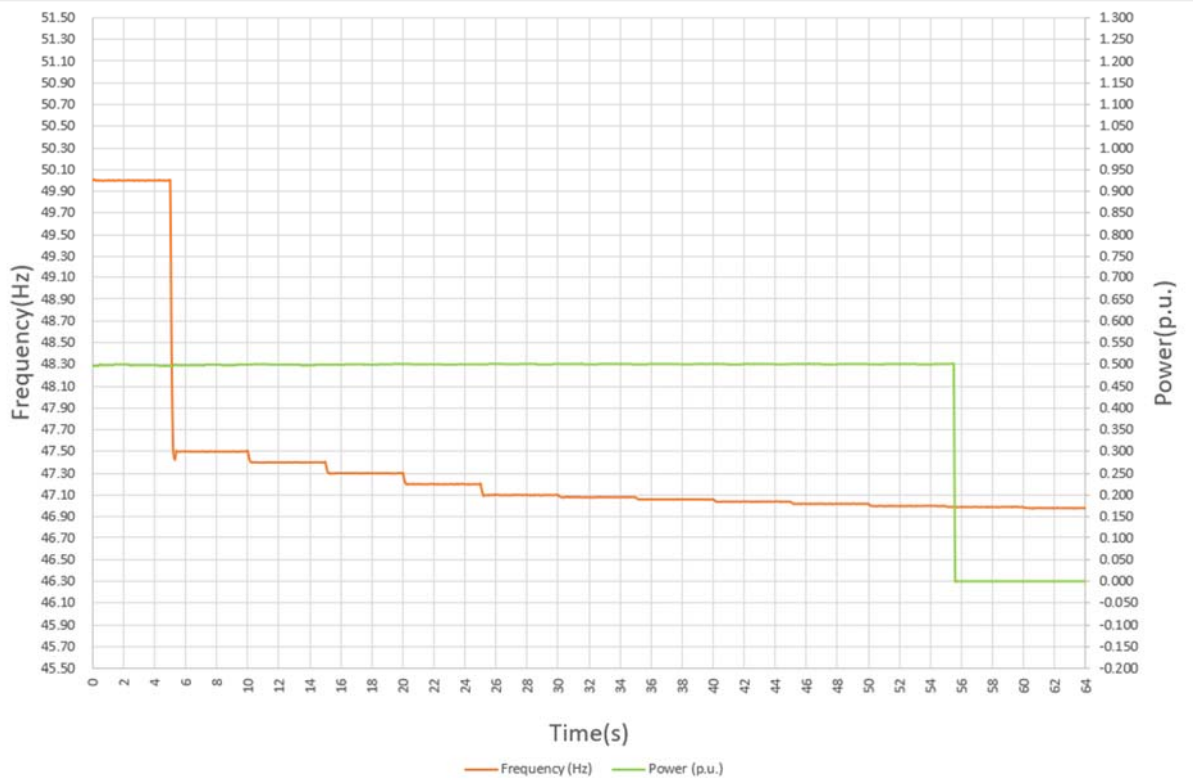




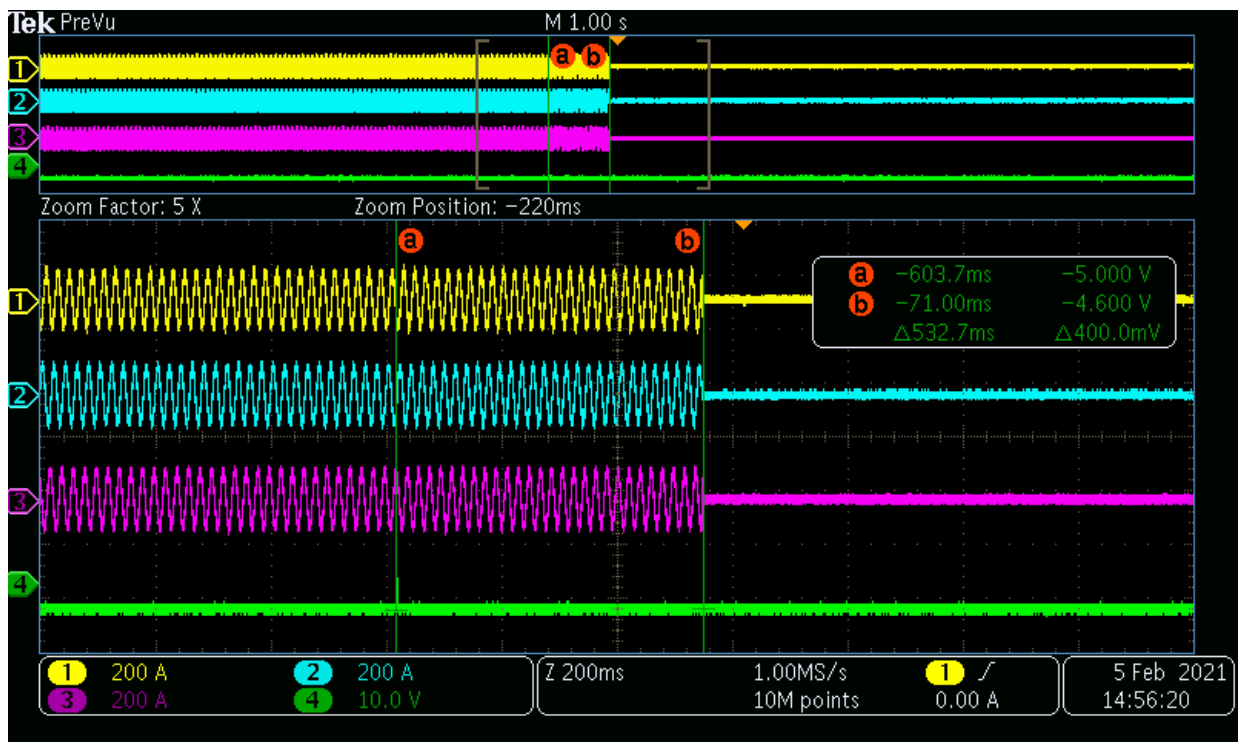
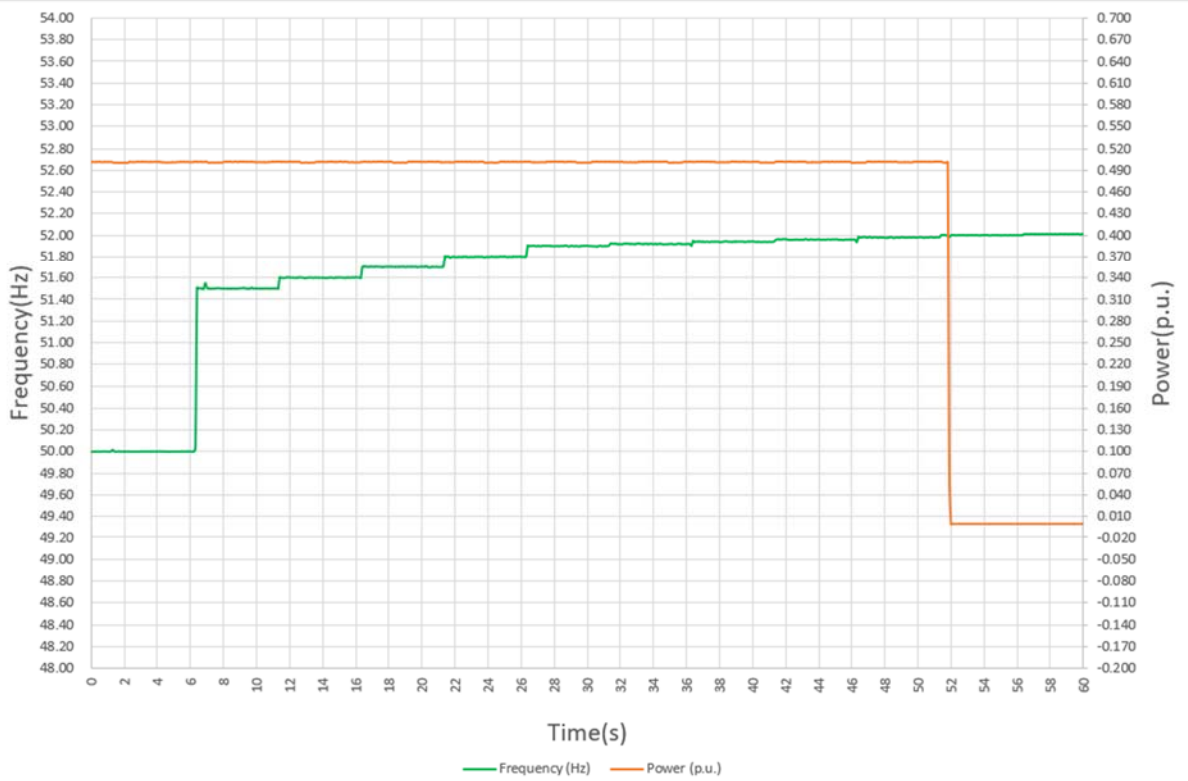
U/F stage 2-4



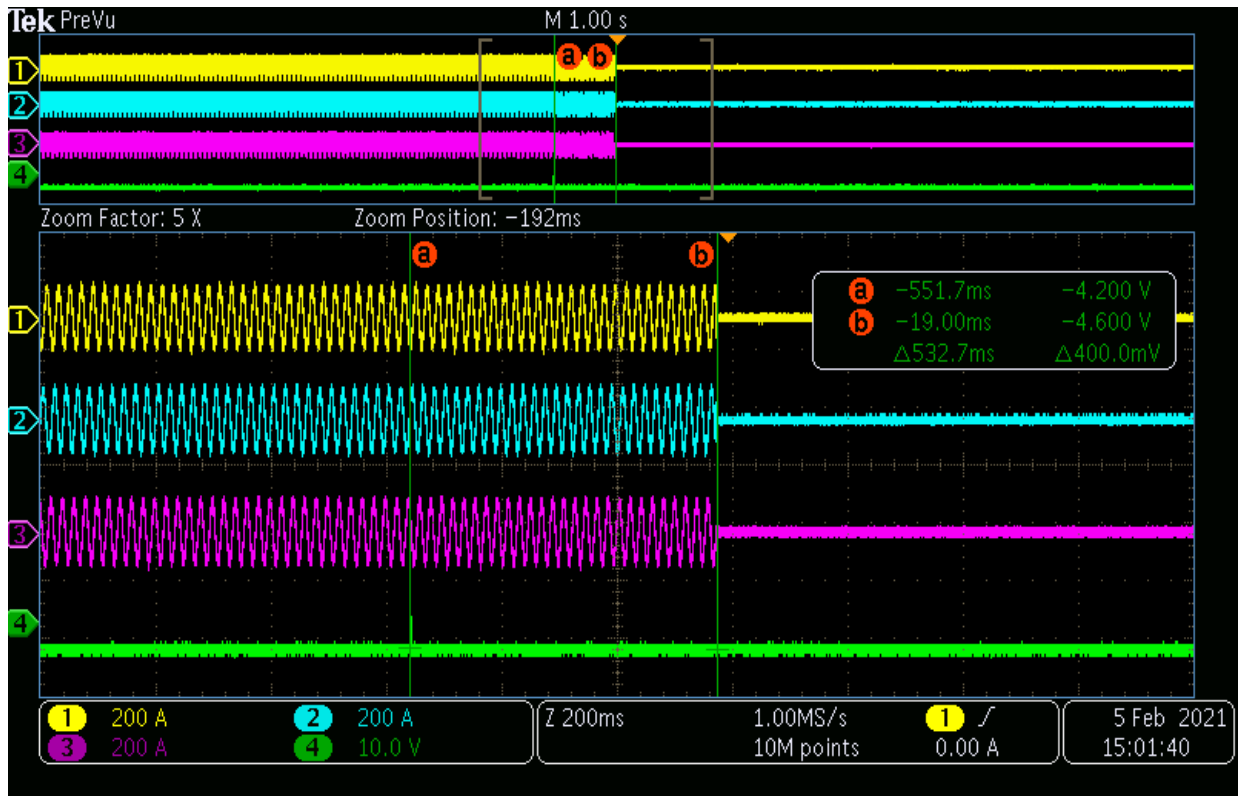
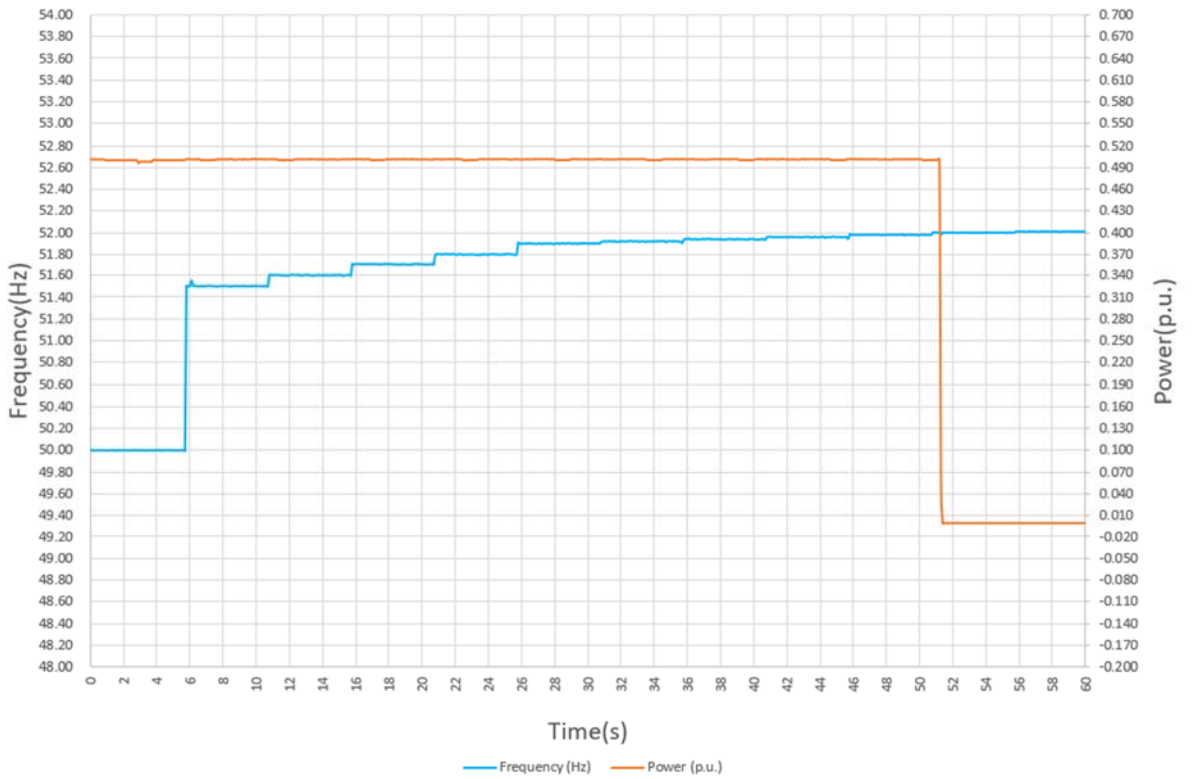
U/F stage 2-5



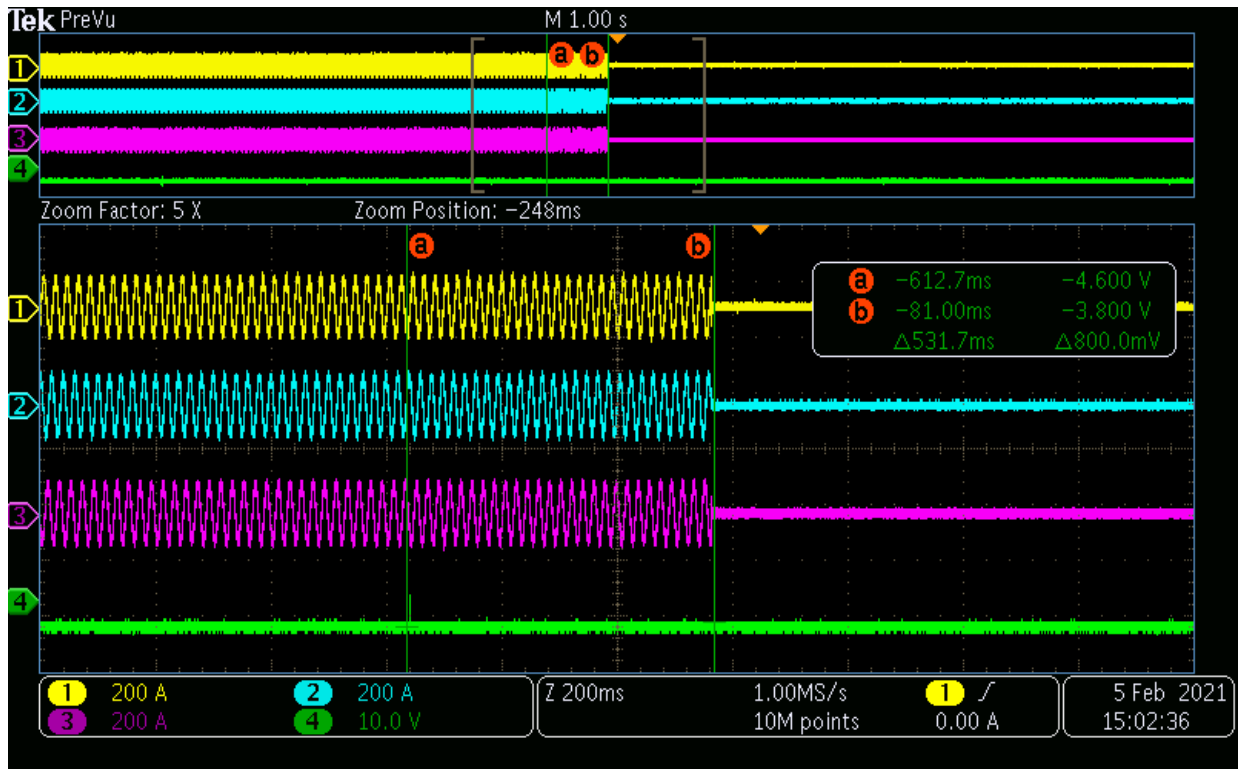
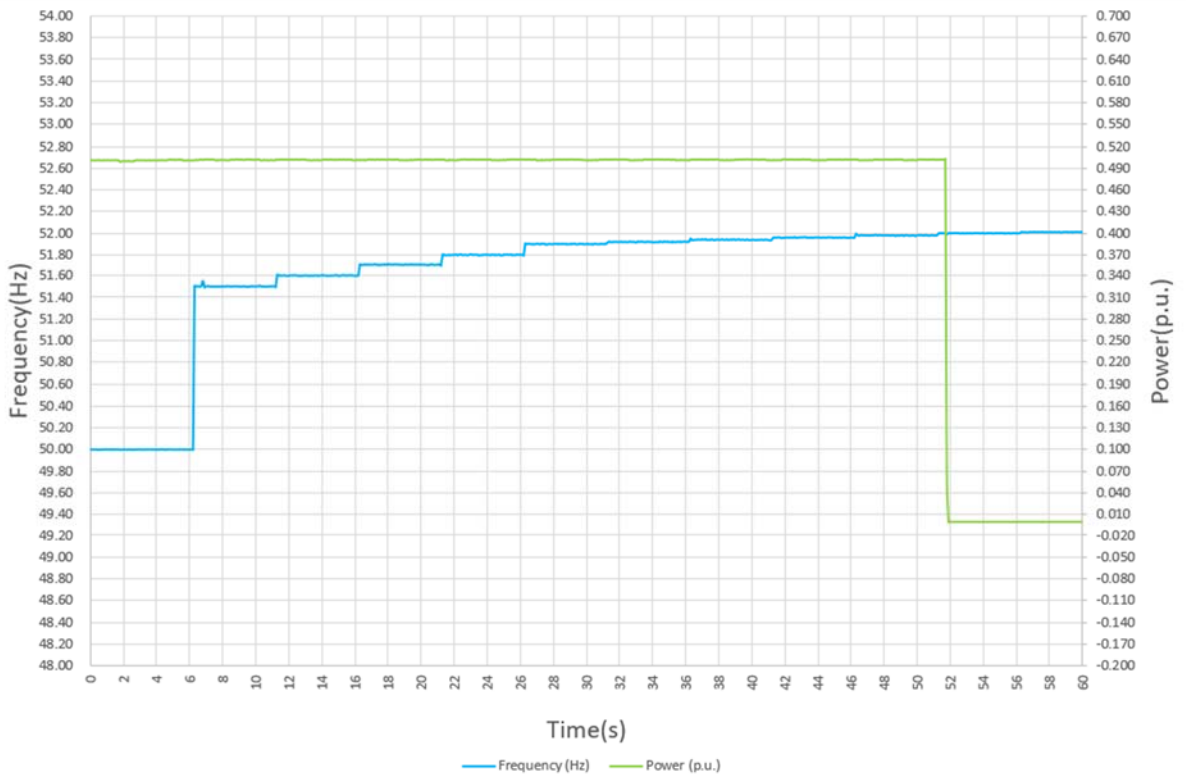
O/F stage 1-1



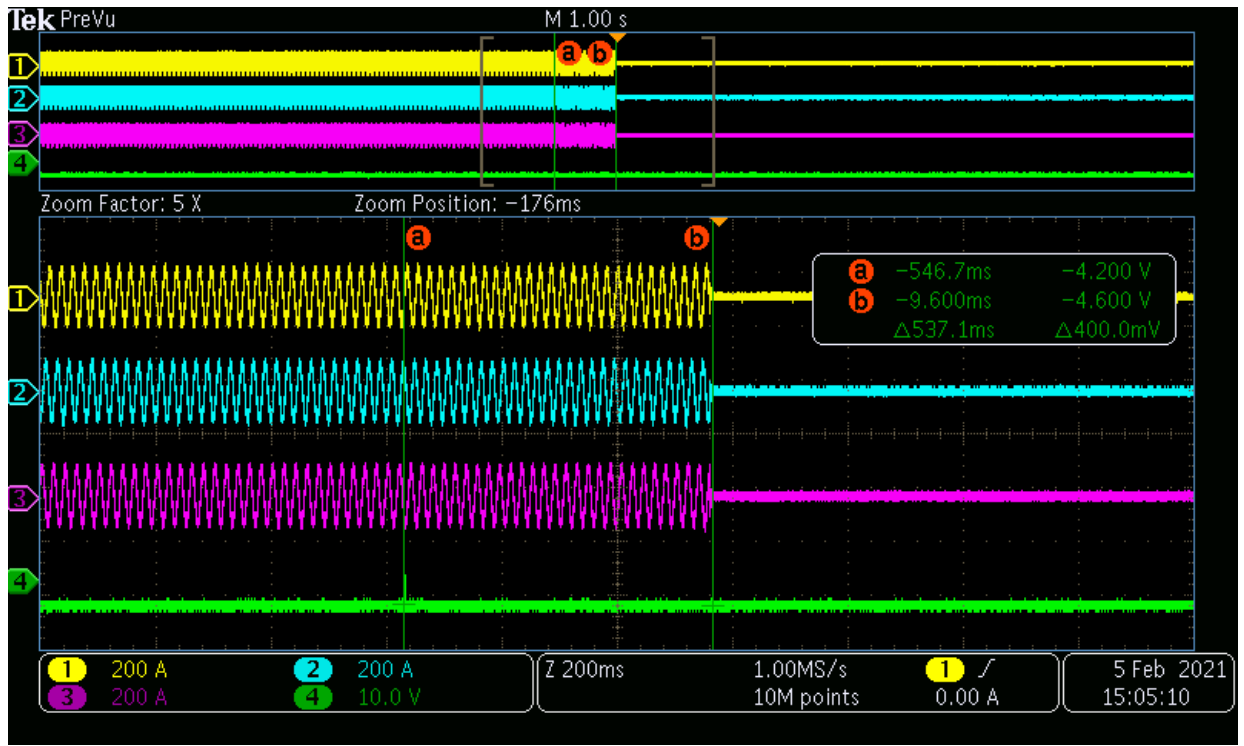
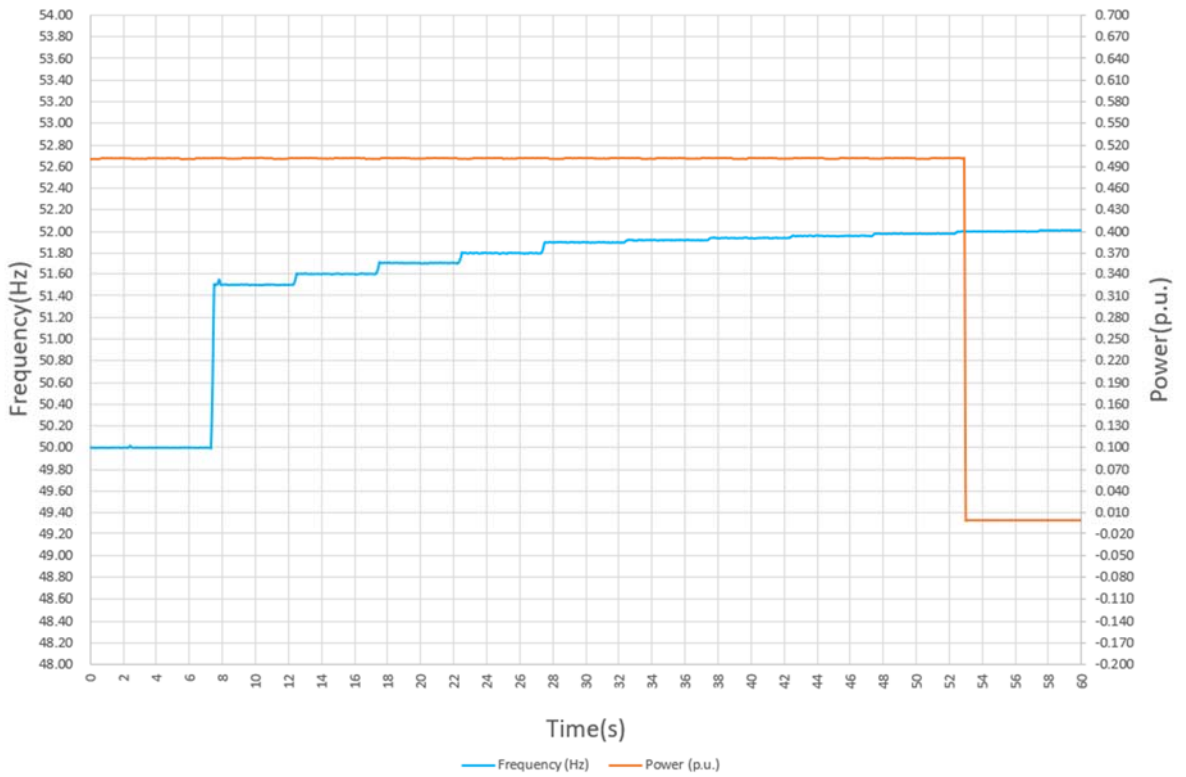
O/F stage 1-2

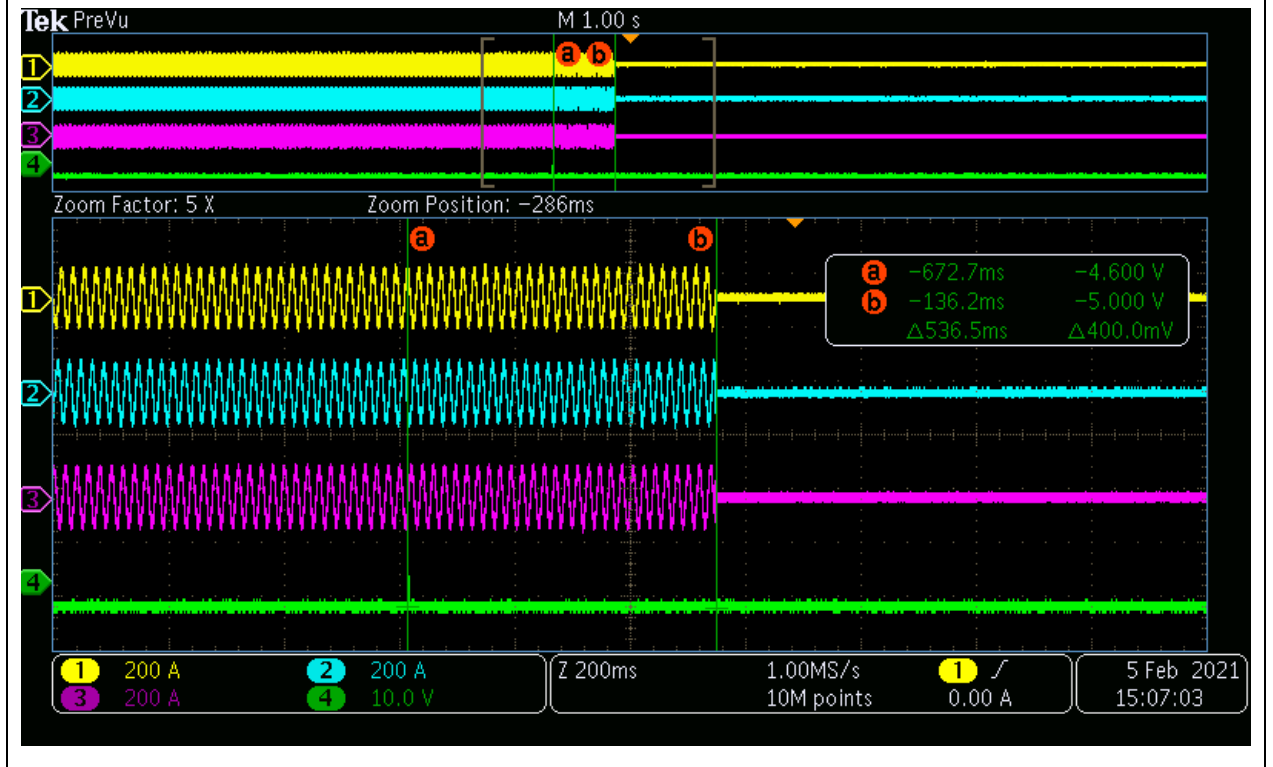
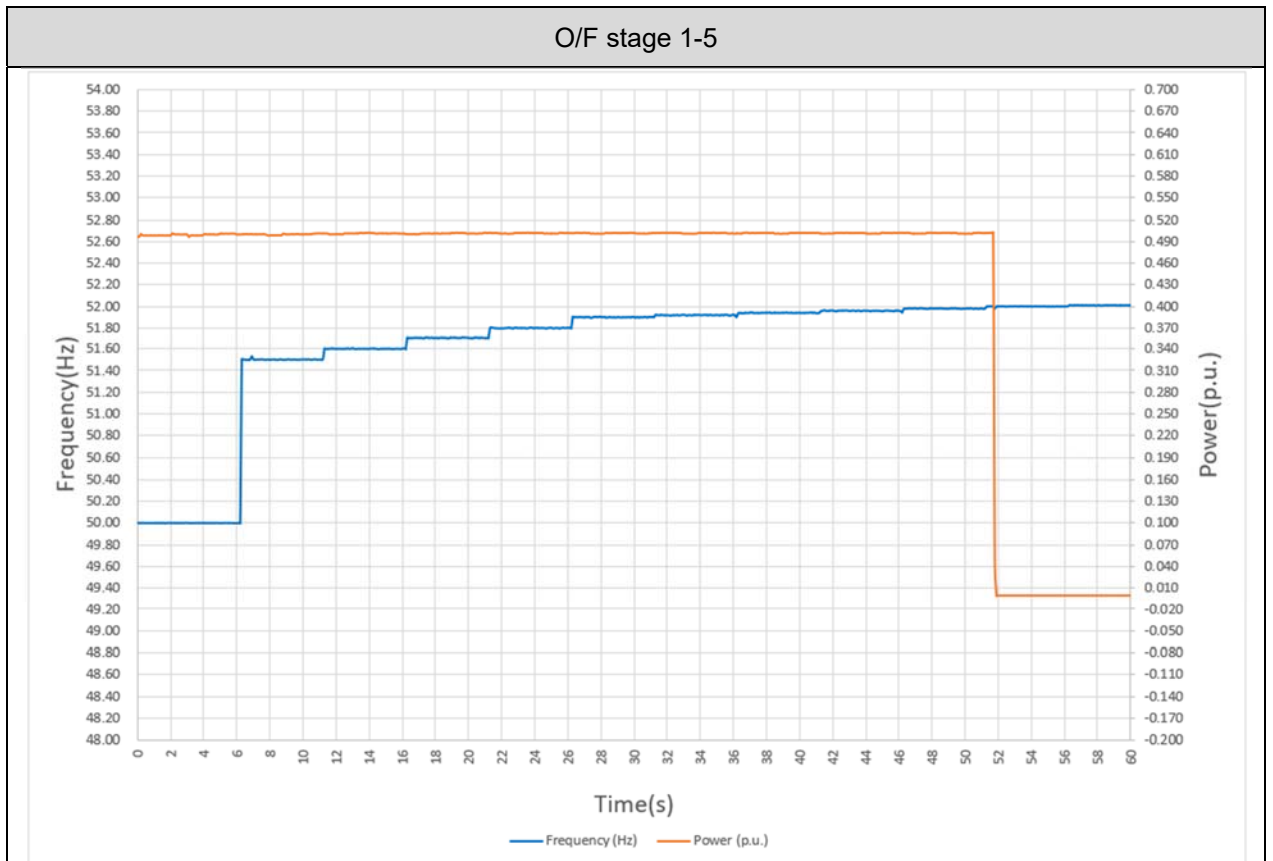


O/F stage 1-3

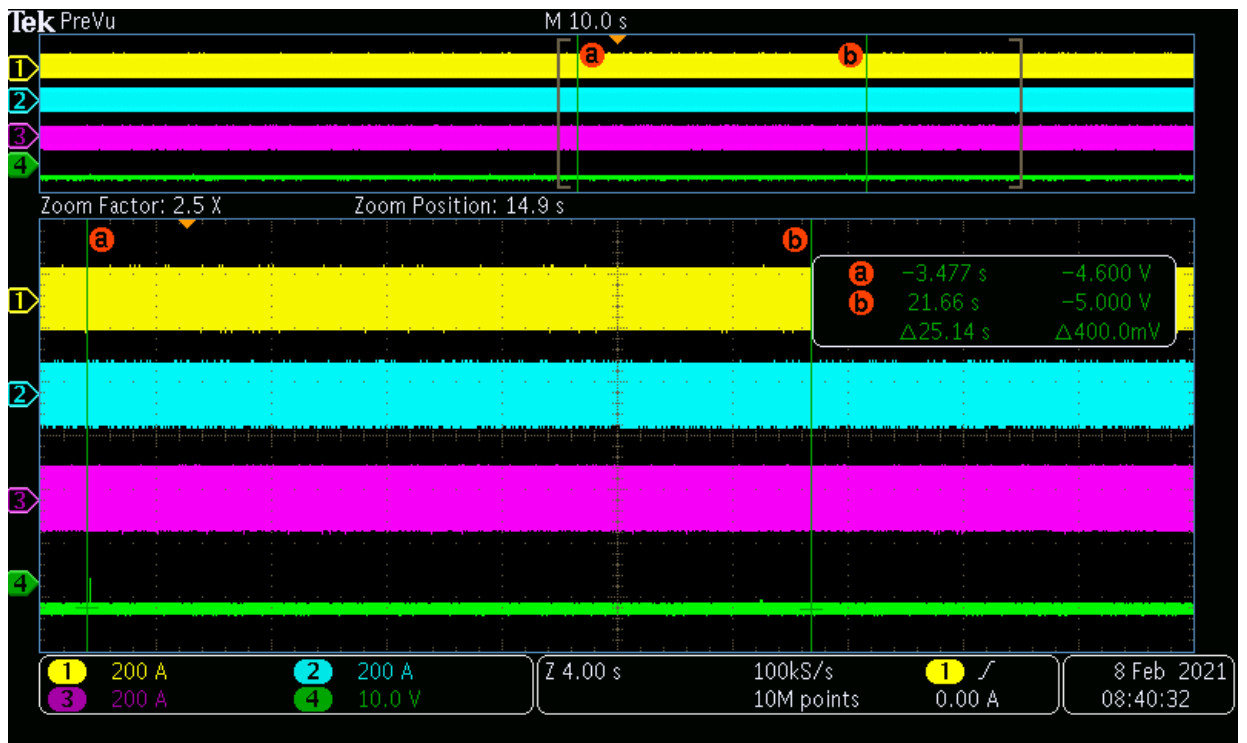
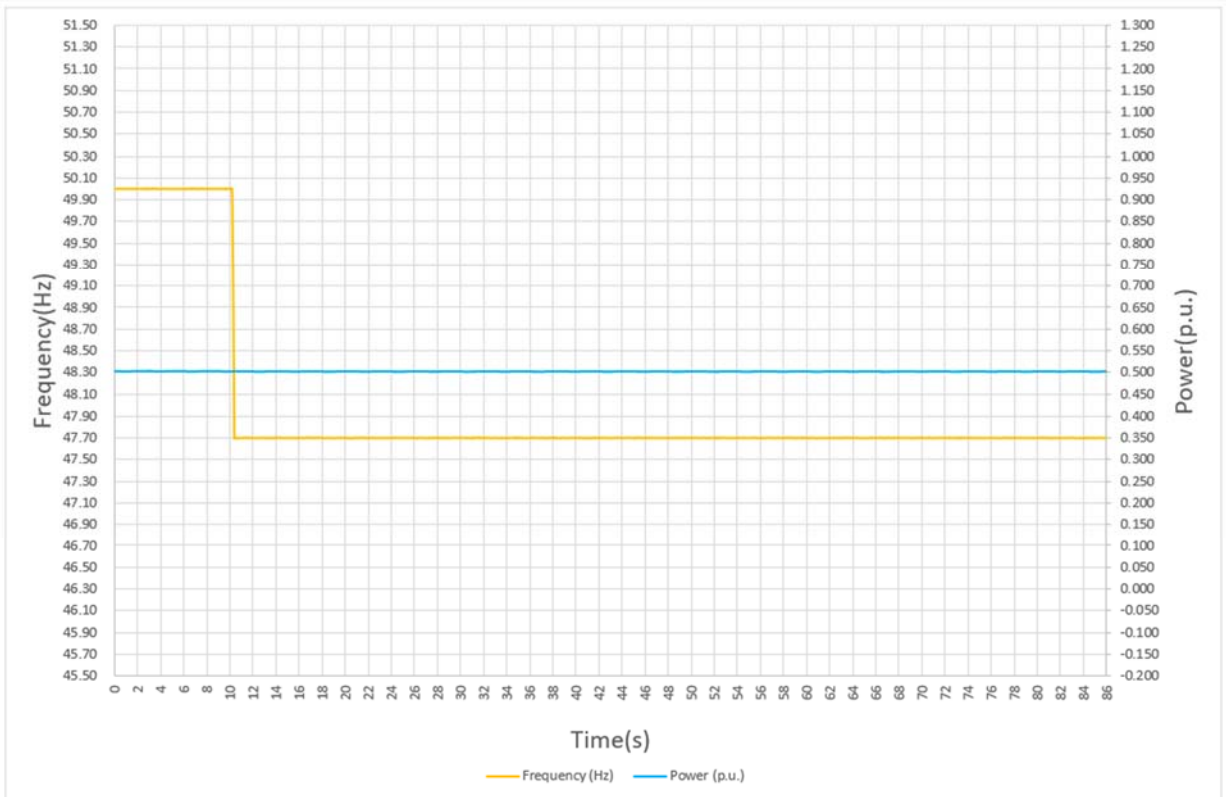


O/F stage 1-4



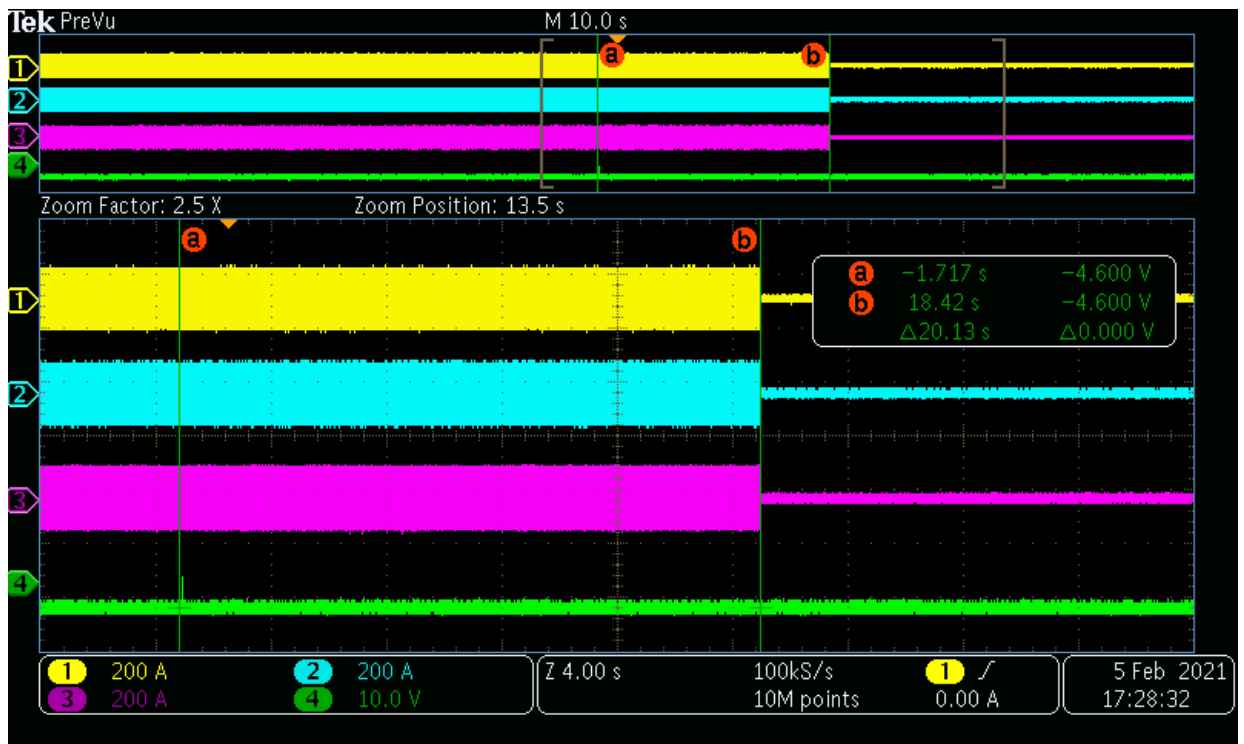
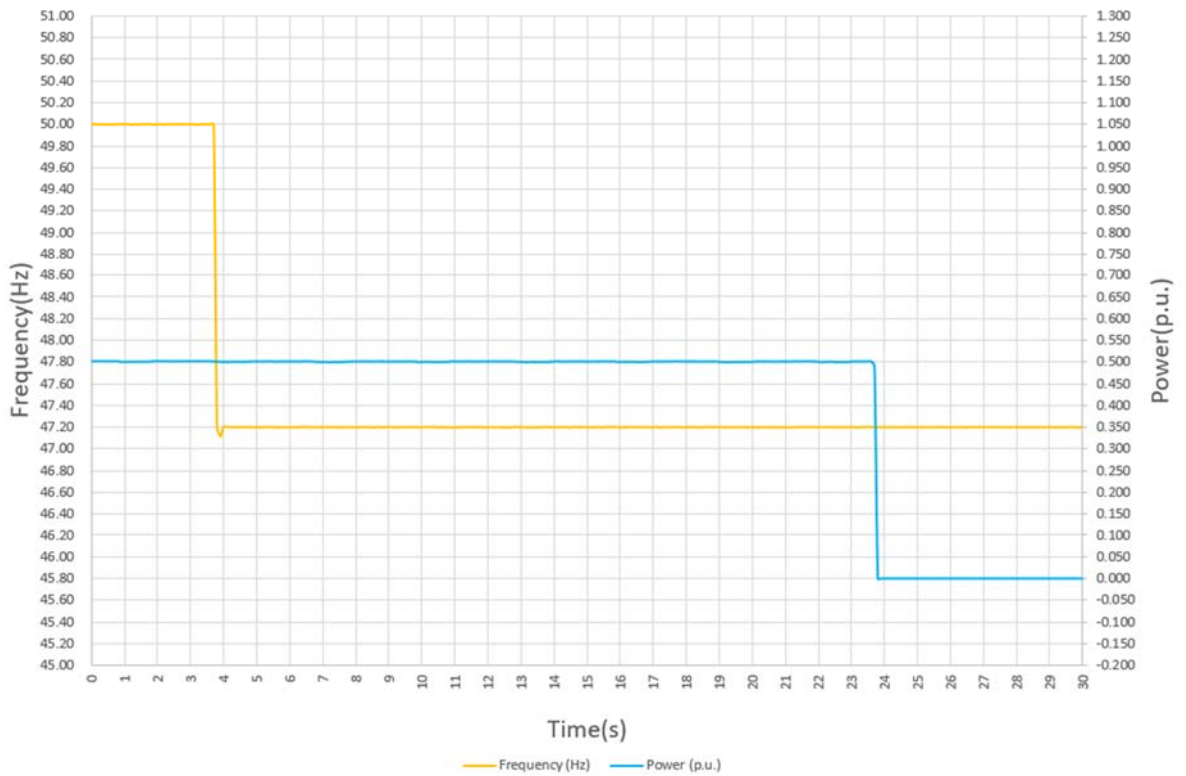


No trip tests - 47.7Hz

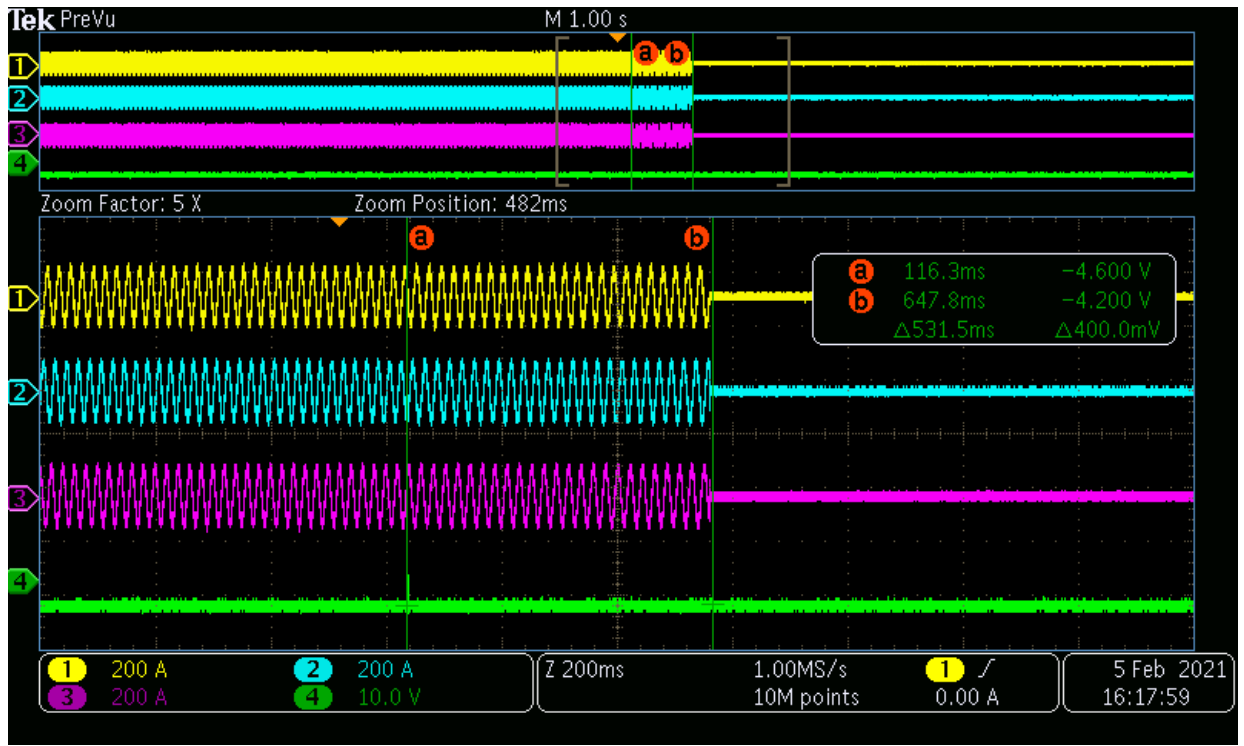
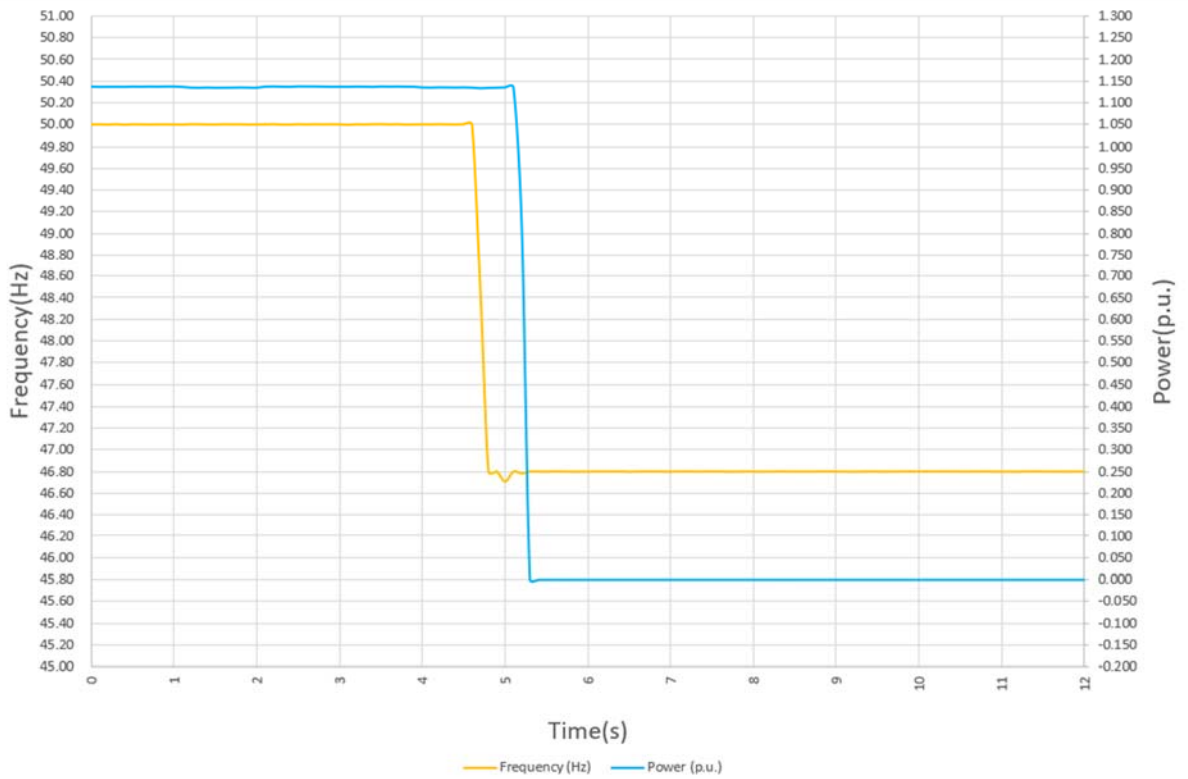




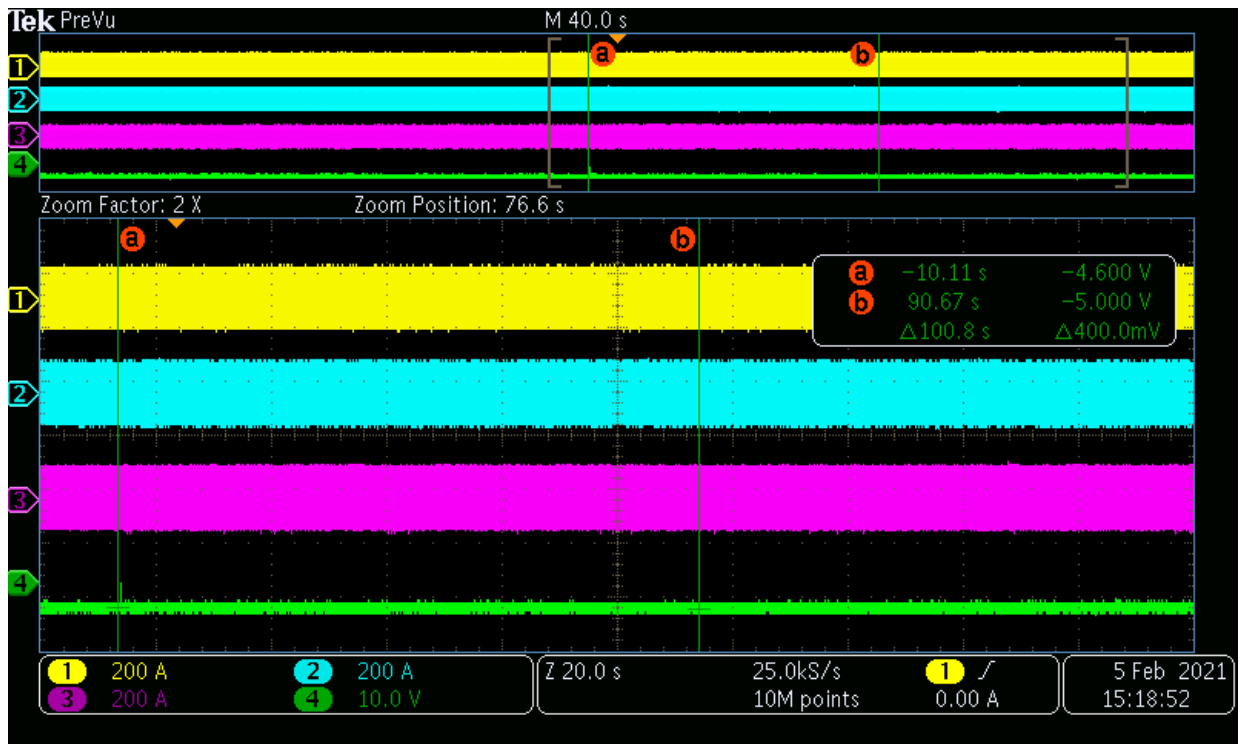
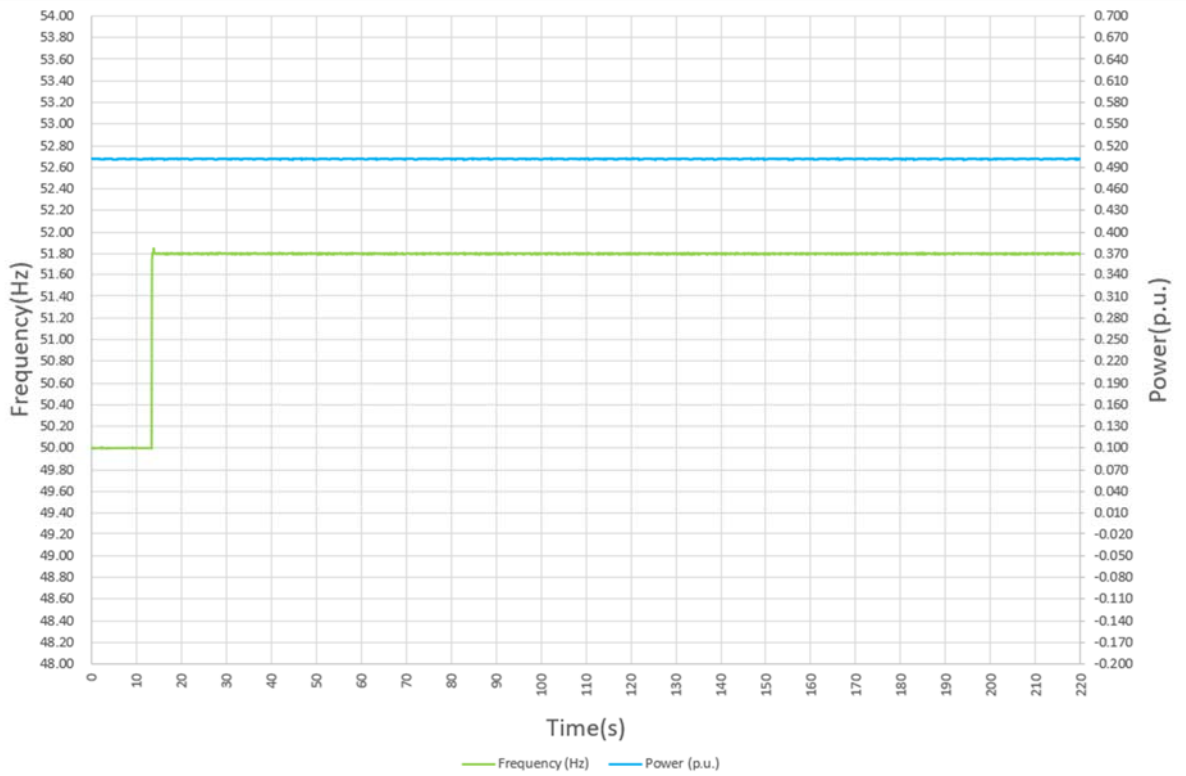
No trip tests – 47.2Hz



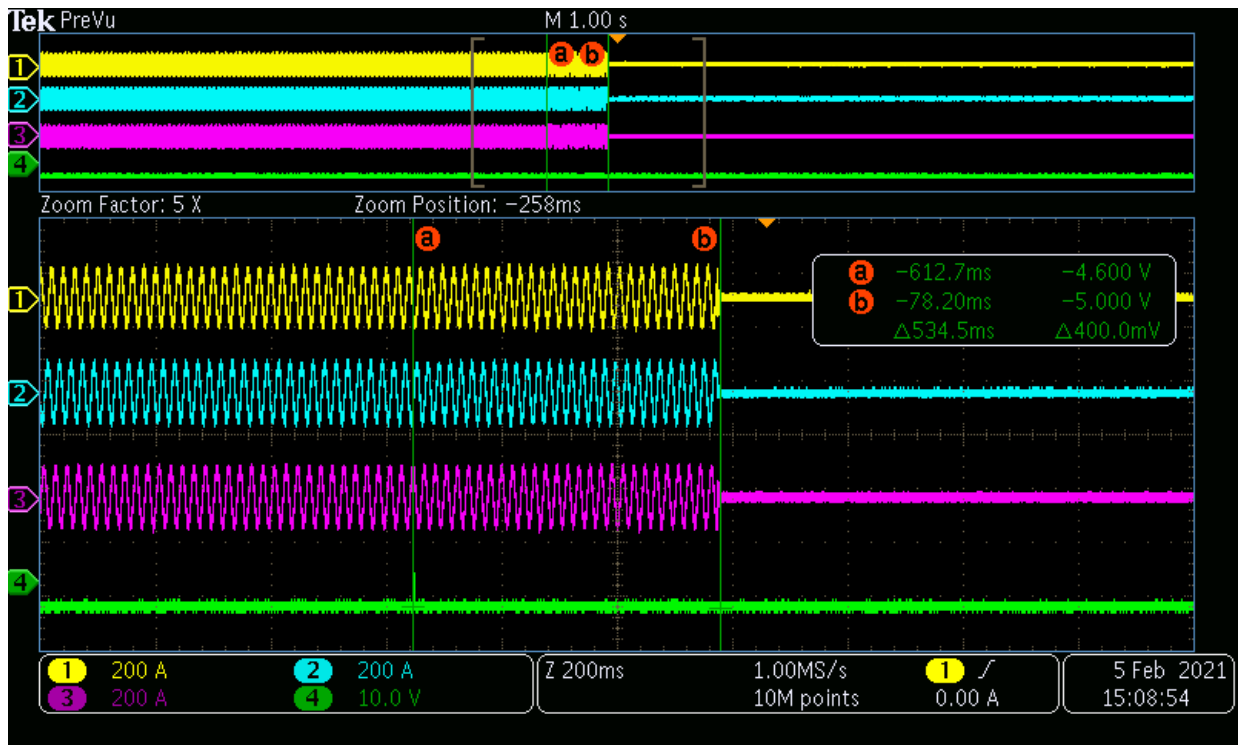
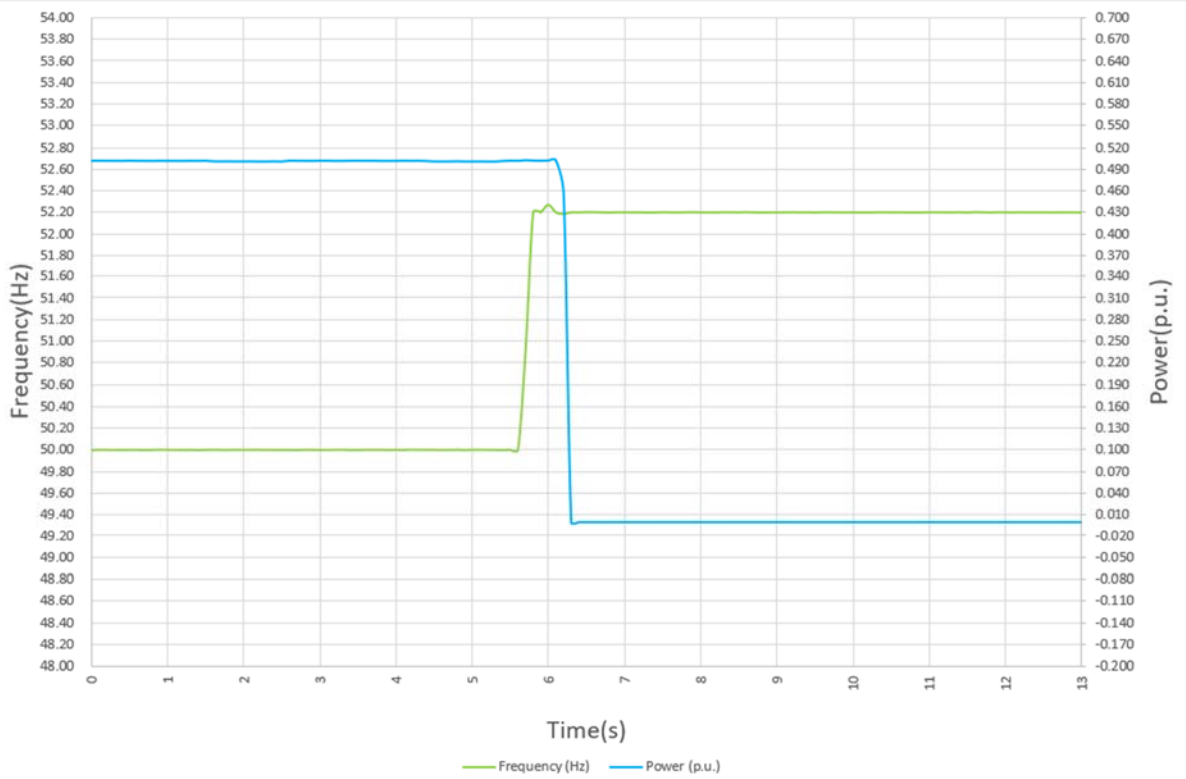
No trip tests – 46.8Hz



No trip tests - 51.8Hz



No trip tests – 52.2Hz



#### 4.3.2 Voltage tests

These tests should be carried out in accordance with Annex A.7.1.2.2.

To establish the certified trip voltage, the test voltage should be applied in steps of  $\pm 0.5\%$  of setting for a duration that is longer than the trip time delay.

To establish the certified trip time, the test voltage should be applied starting from  $\pm 1.8\%$  below the certified trip voltage in a step of at least  $\pm 0.5\%$  of setting for a duration that is longer than the trip time delay. For each trip setting five tests shall be carried out.

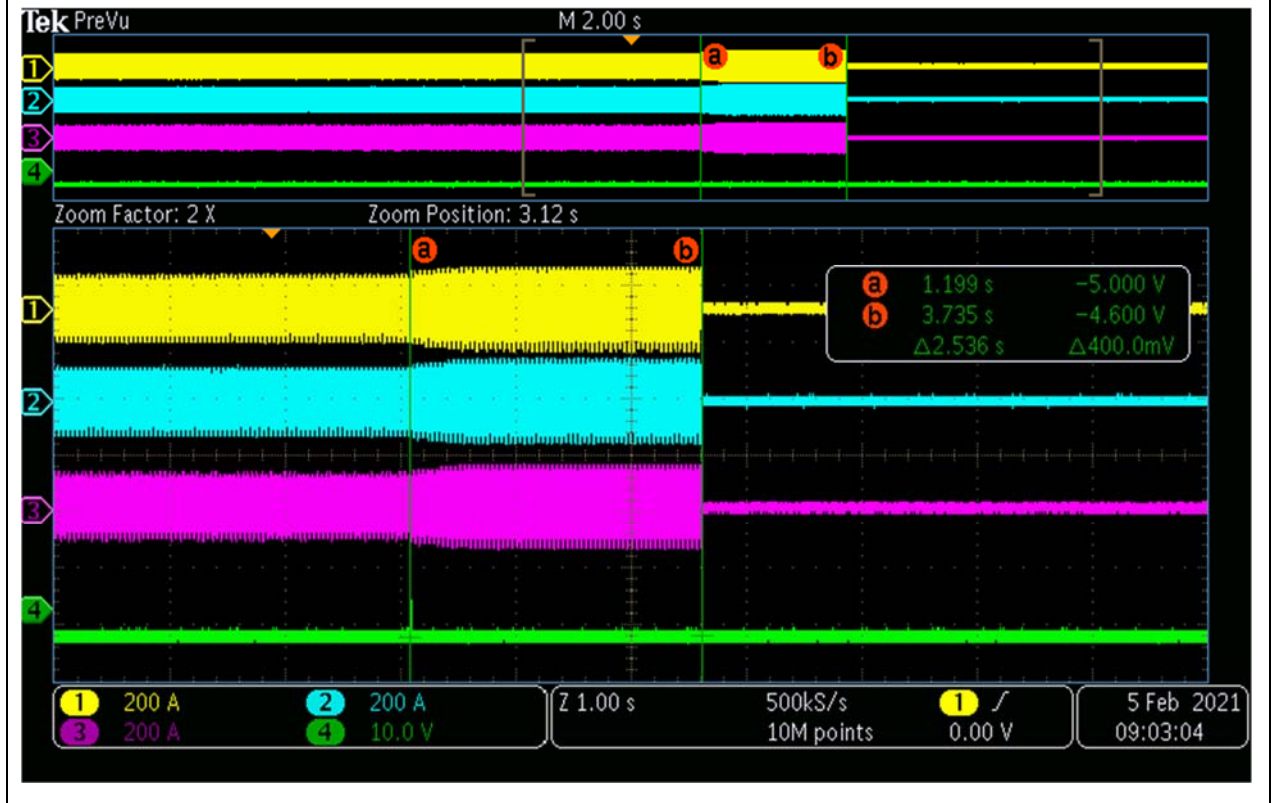
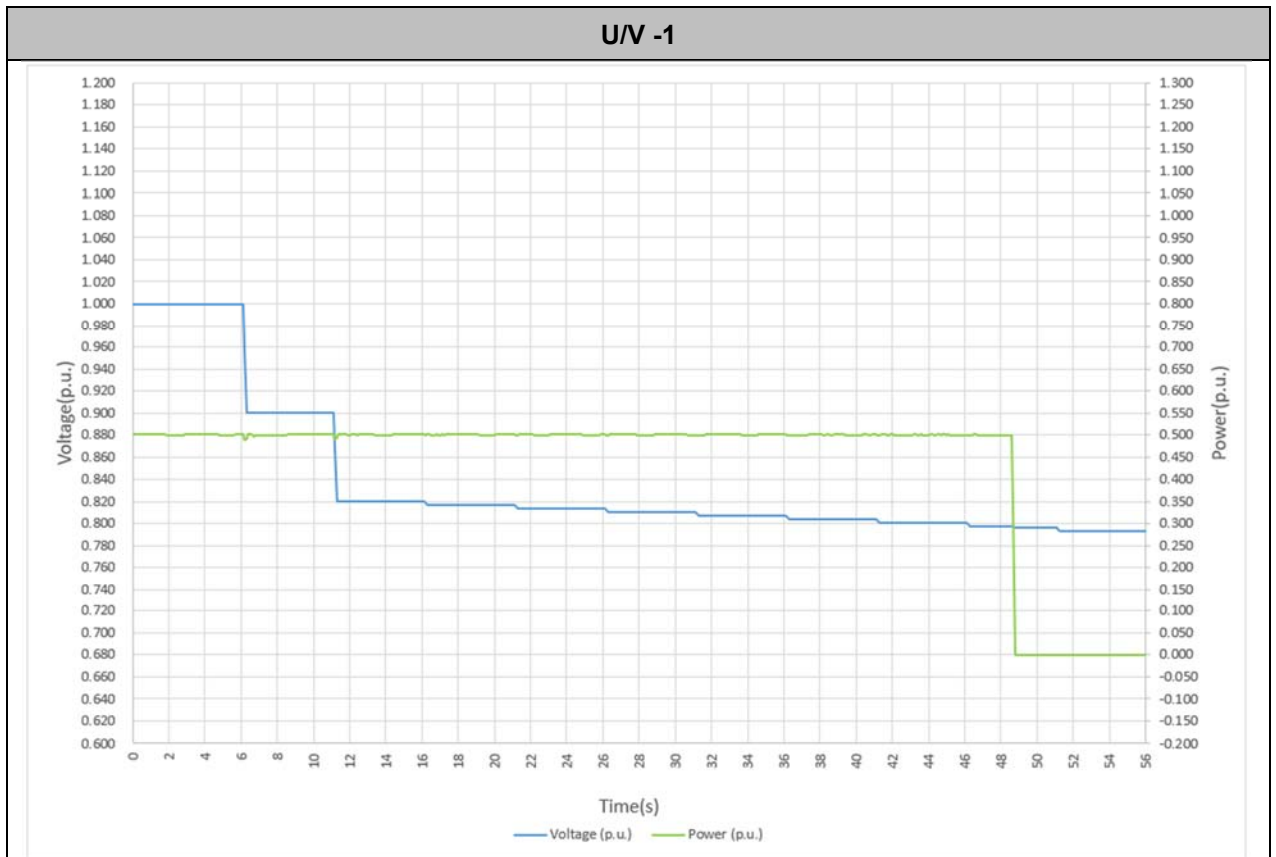
Following tables show the test results:

Function	Setting		Trip test		"No trip tests"	
	Voltage	Time delay	Voltage (V)	Time delay (s)	Voltage /time	Confirm no trip
U/V	249.4 V	2.5 s	248.9	2.536	254.9 V / 3.50 s	Pass
			248.9	2.530		
			248.9	2.542		
			248.9	2.532		
			249.0	2.538		
					244 V / 2.48 s	Pass
O/V stage 1	355.4 V	1.0 s	356.0	1.021	350V / 2.0 s	Pass
			355.9	1.029		
			356.0	1.033		
			356.0	1.025		
			356.0	1.033		
O/V stage 2	371.0 V	0.5 s	374.6	0.535	365.6 V / 0.98 s	Pass
			371.1	0.537		
			371.0	0.531		
			370.9	0.527		
			370.9	0.533		
					376.5 V / 0.48 s	Pass

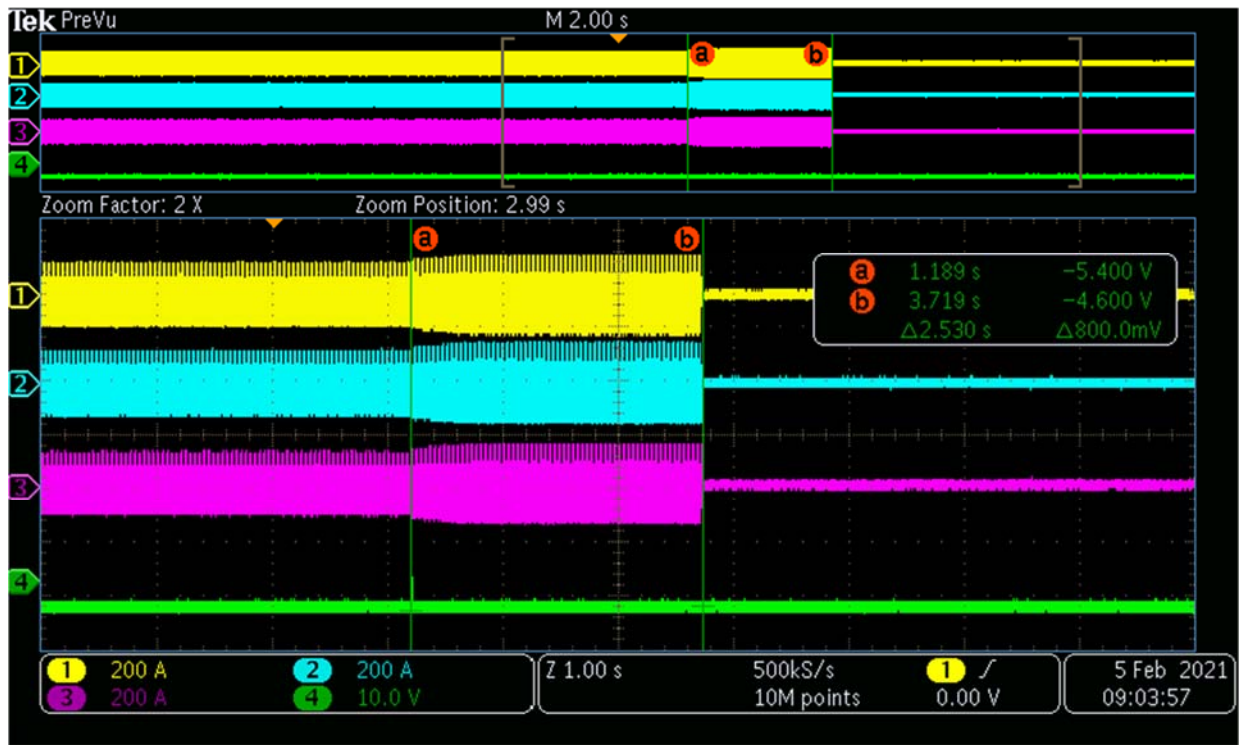
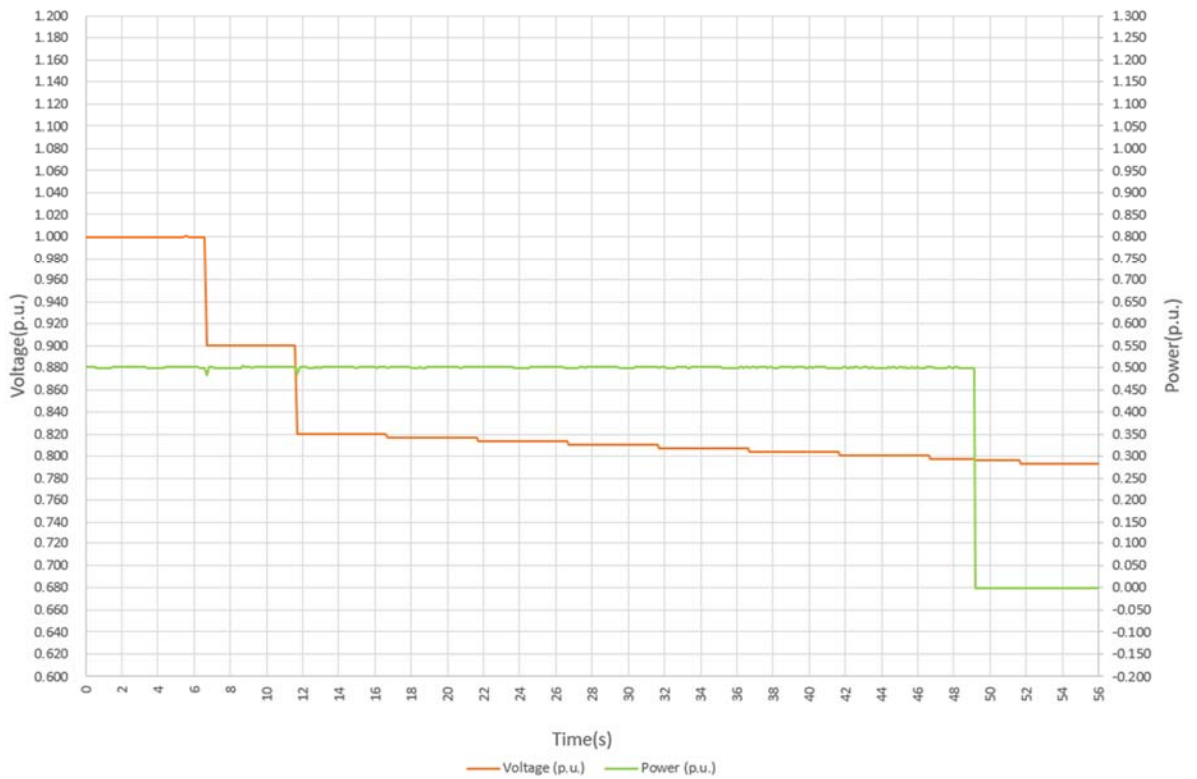
Note for Voltage tests the Voltage required to trip is the setting  $\pm 3.45$  V. The time delay can be measured at a larger deviation than the minimum required to operate the protection. The No trip tests need to be carried out at the setting  $\pm 4$  V and for the relevant times as shown in the table above to ensure that the protection will not trip in error.

Remark: The virtual neutral line was used in the test.

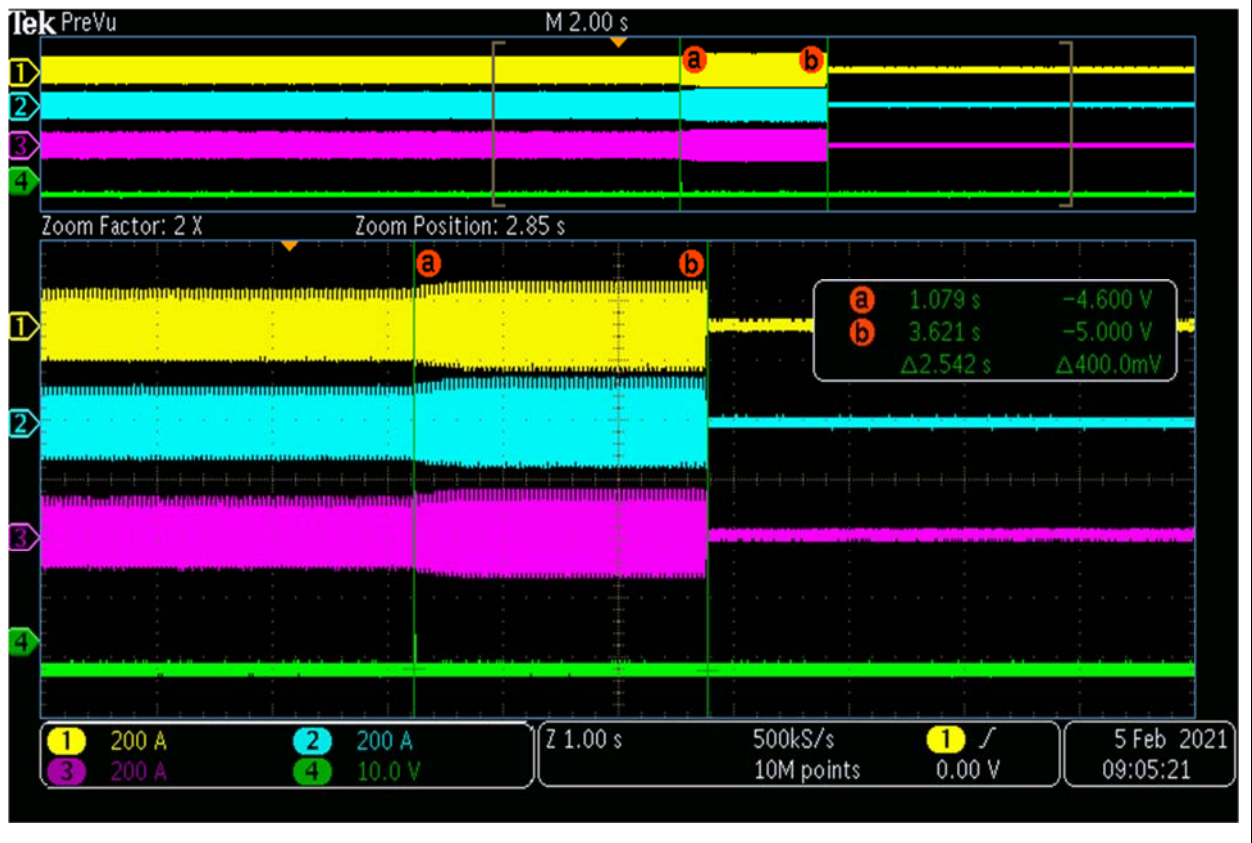
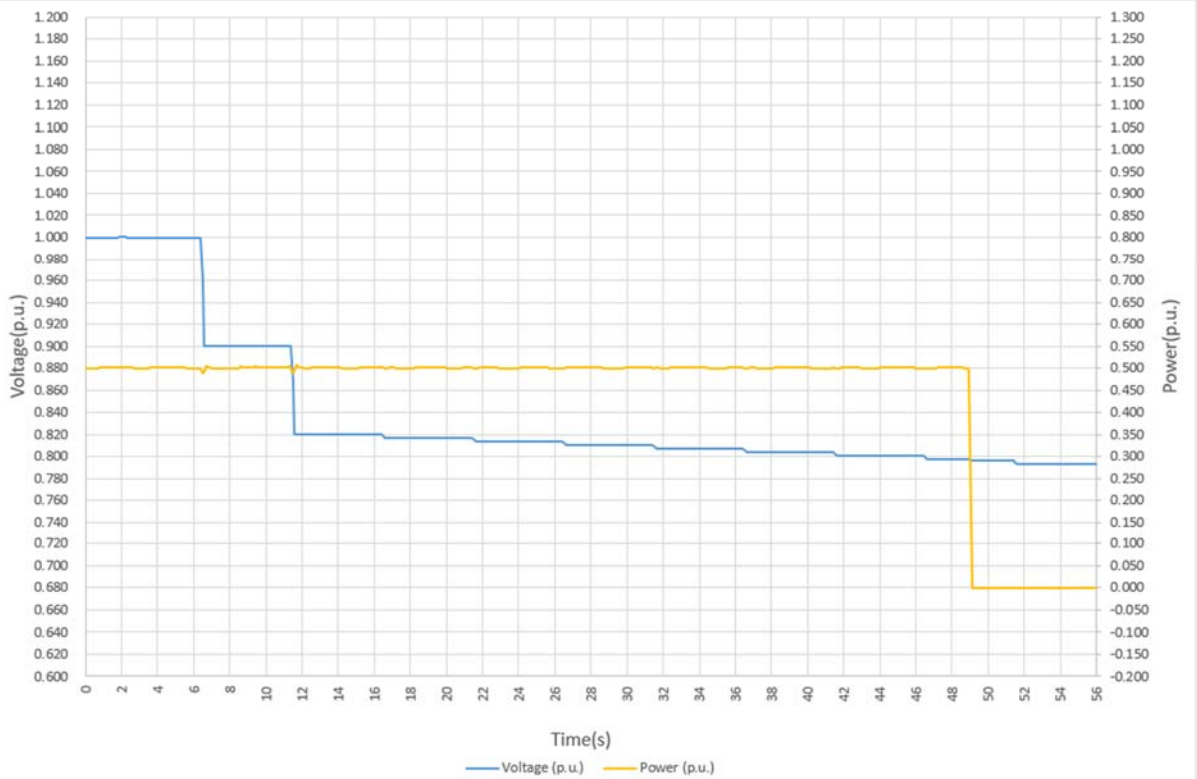
Test results are graphically shown in following pages.



U/V -2

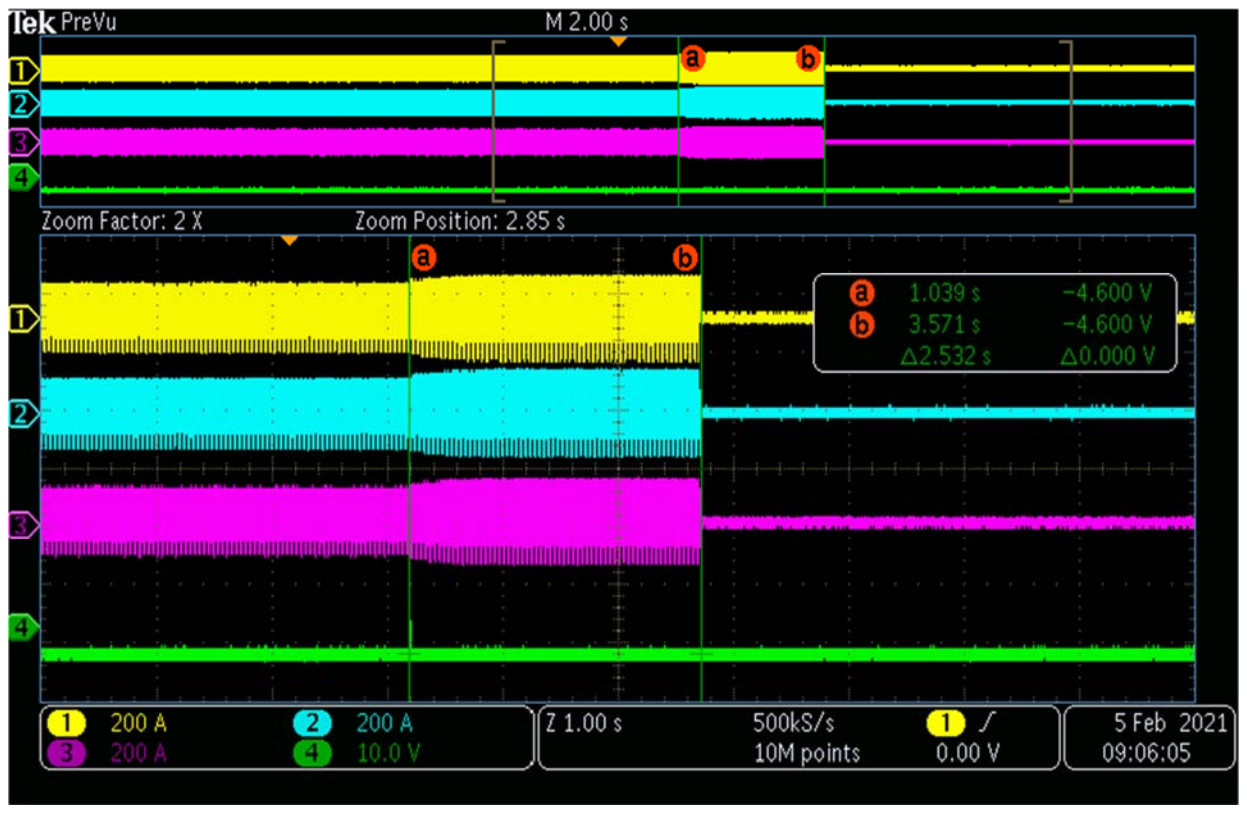
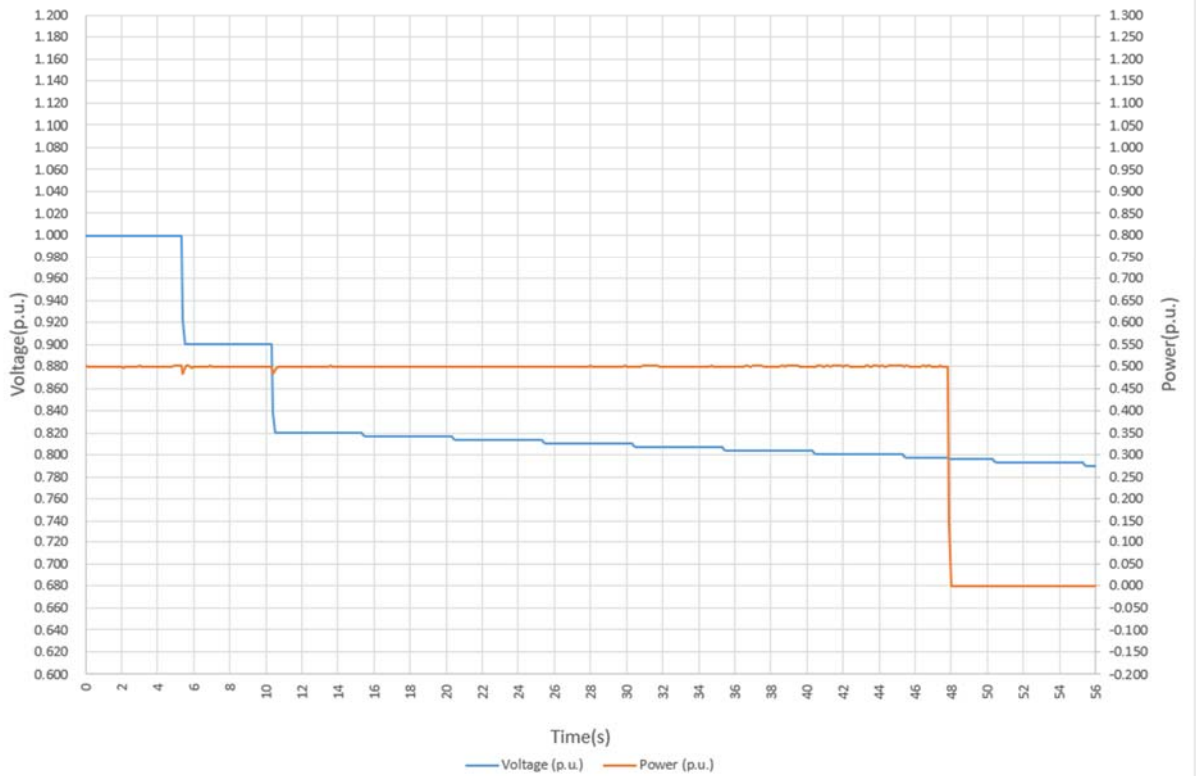


U/V -3

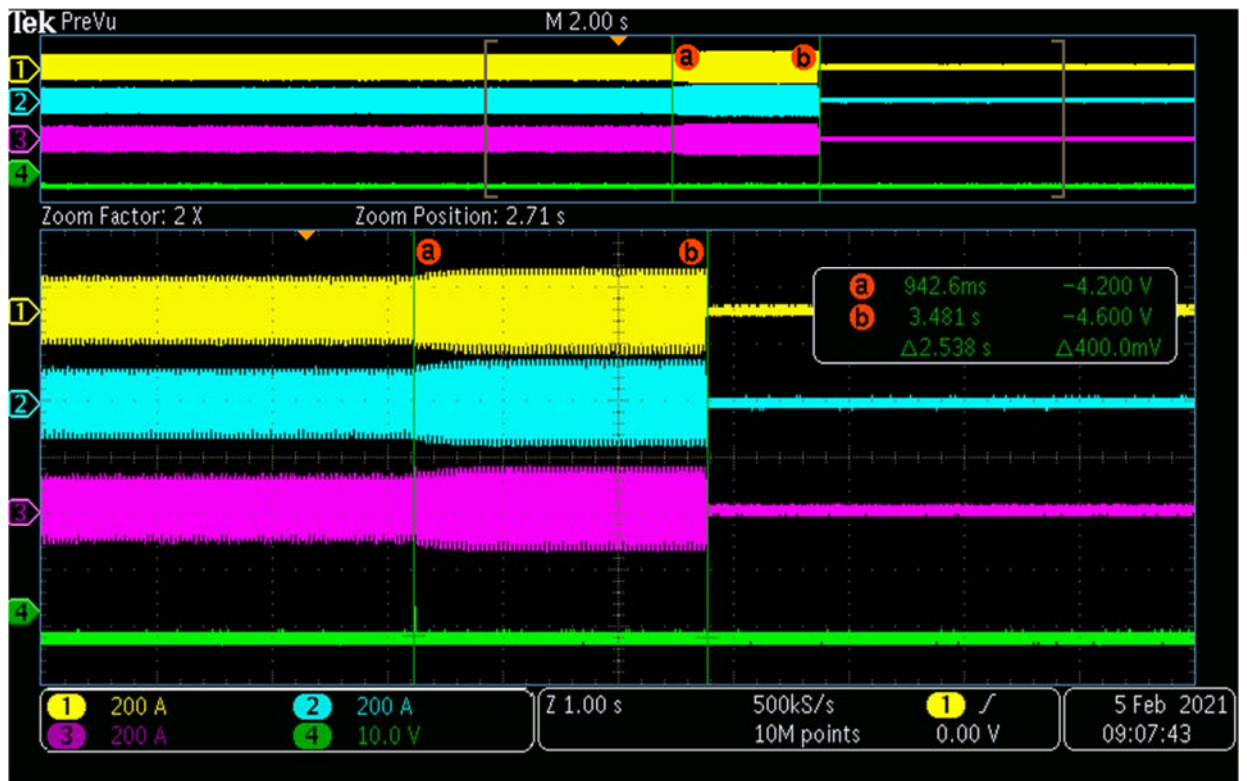
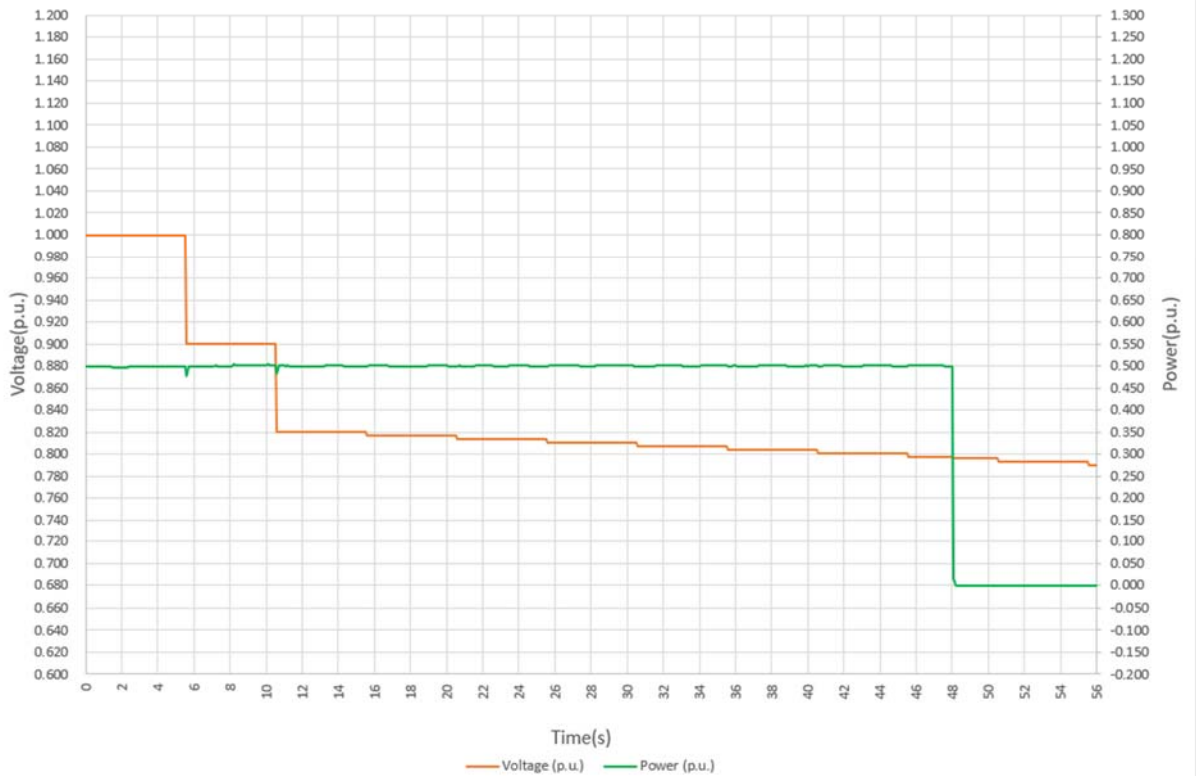




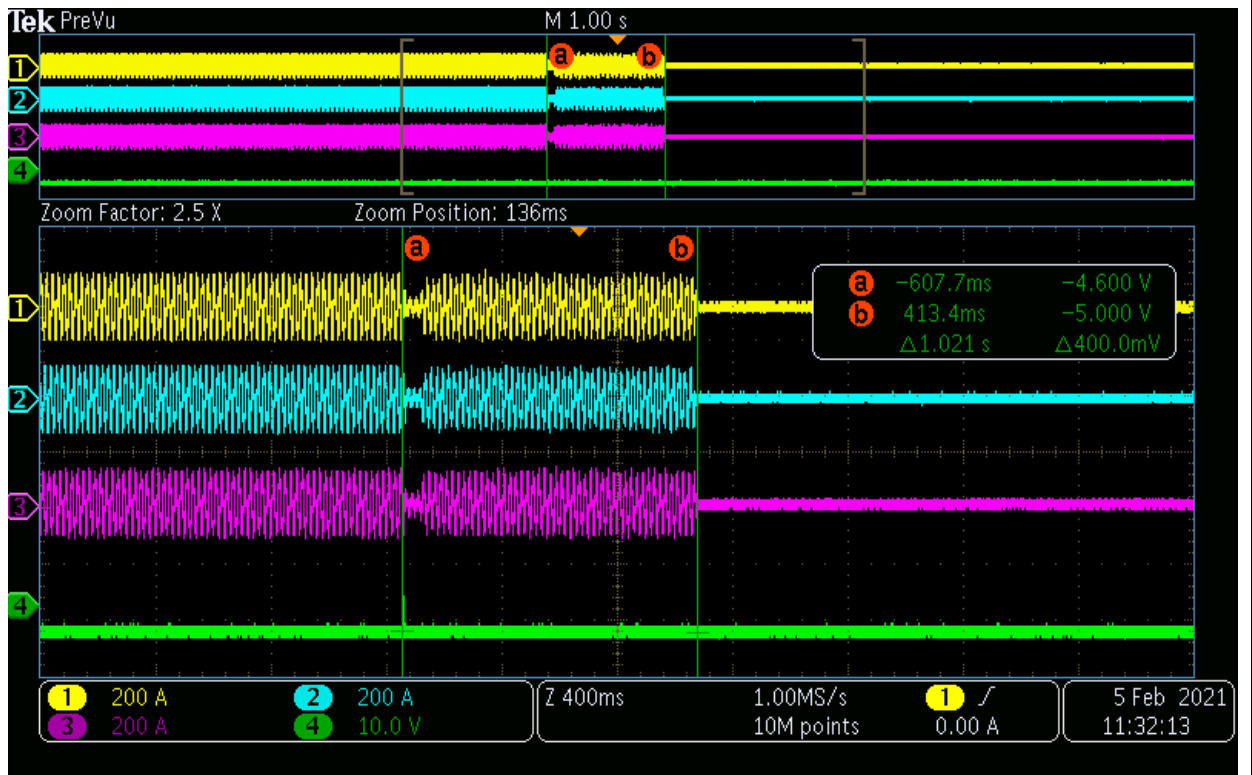
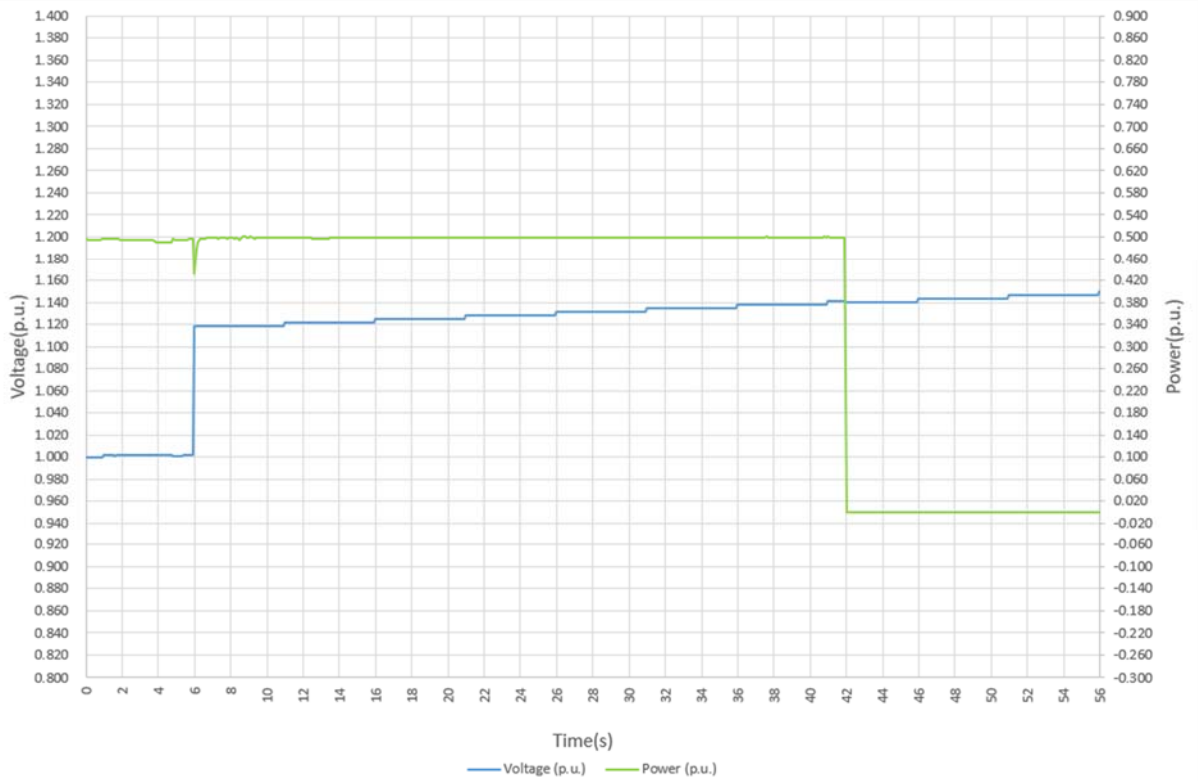
U/V -4



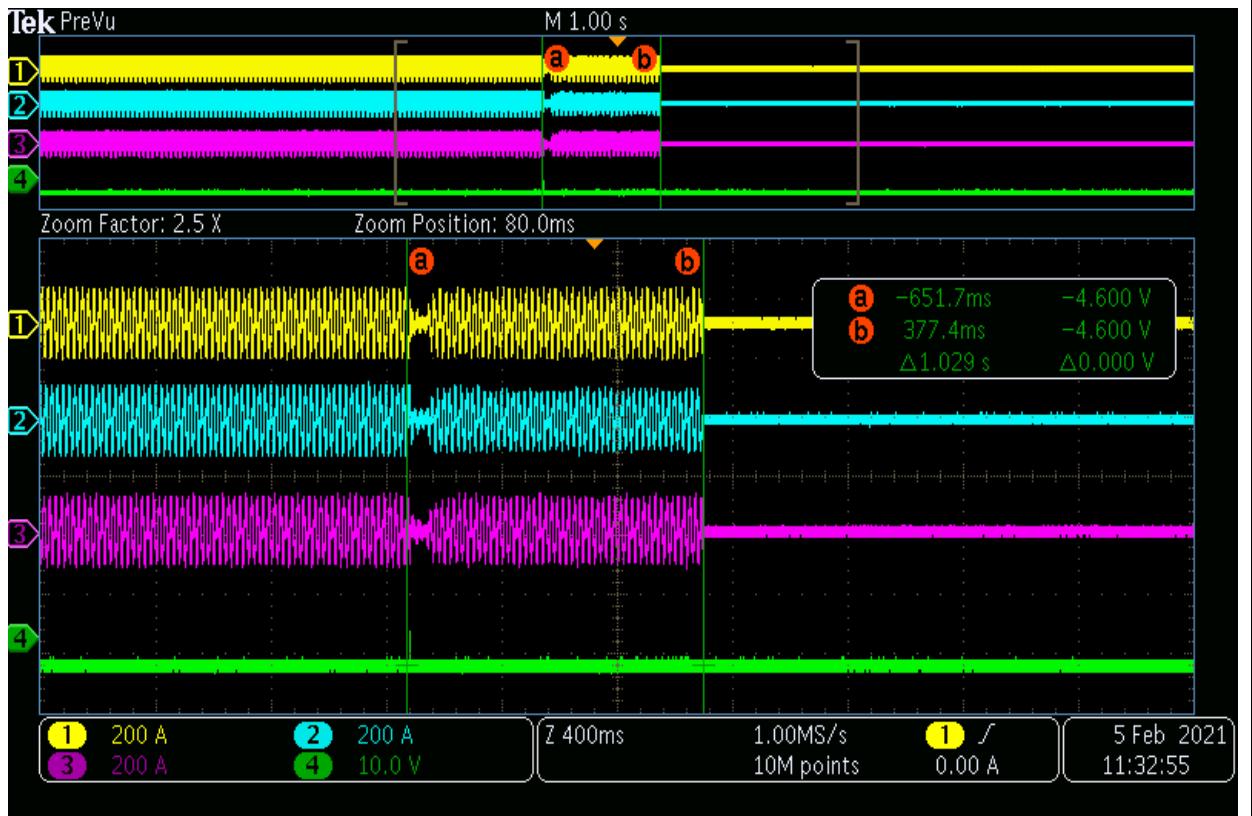
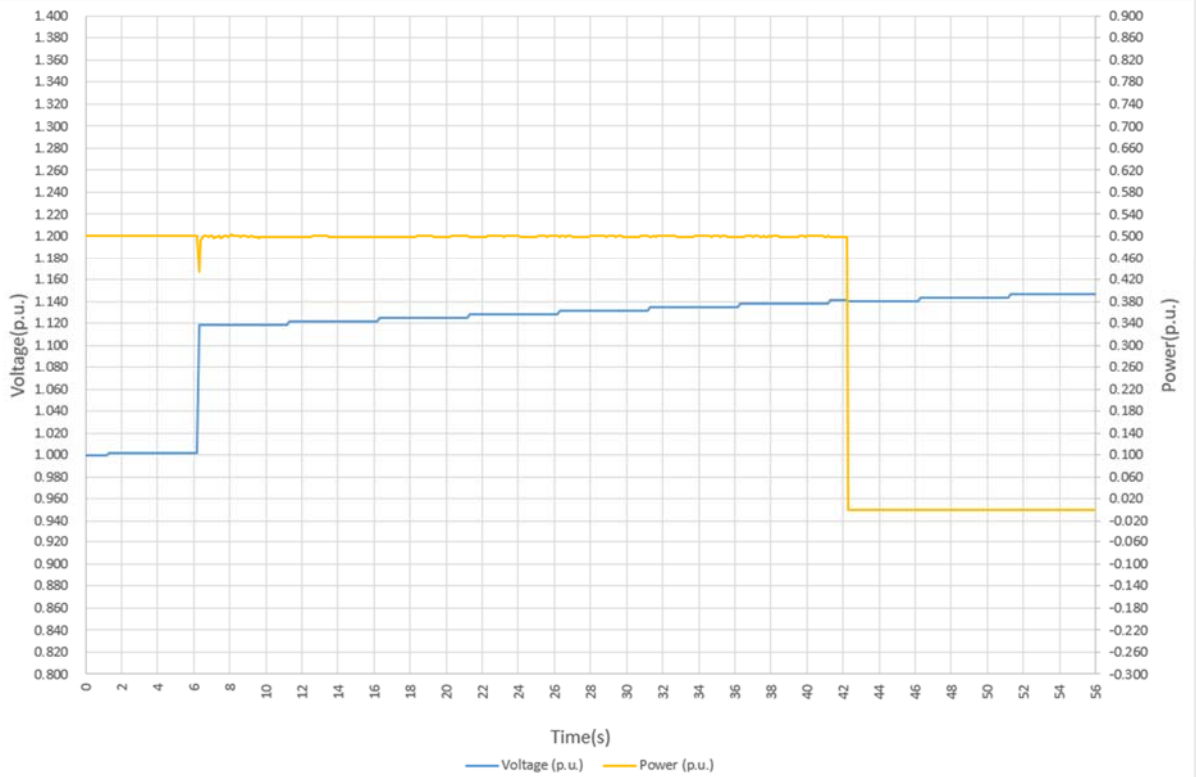
U/V -5



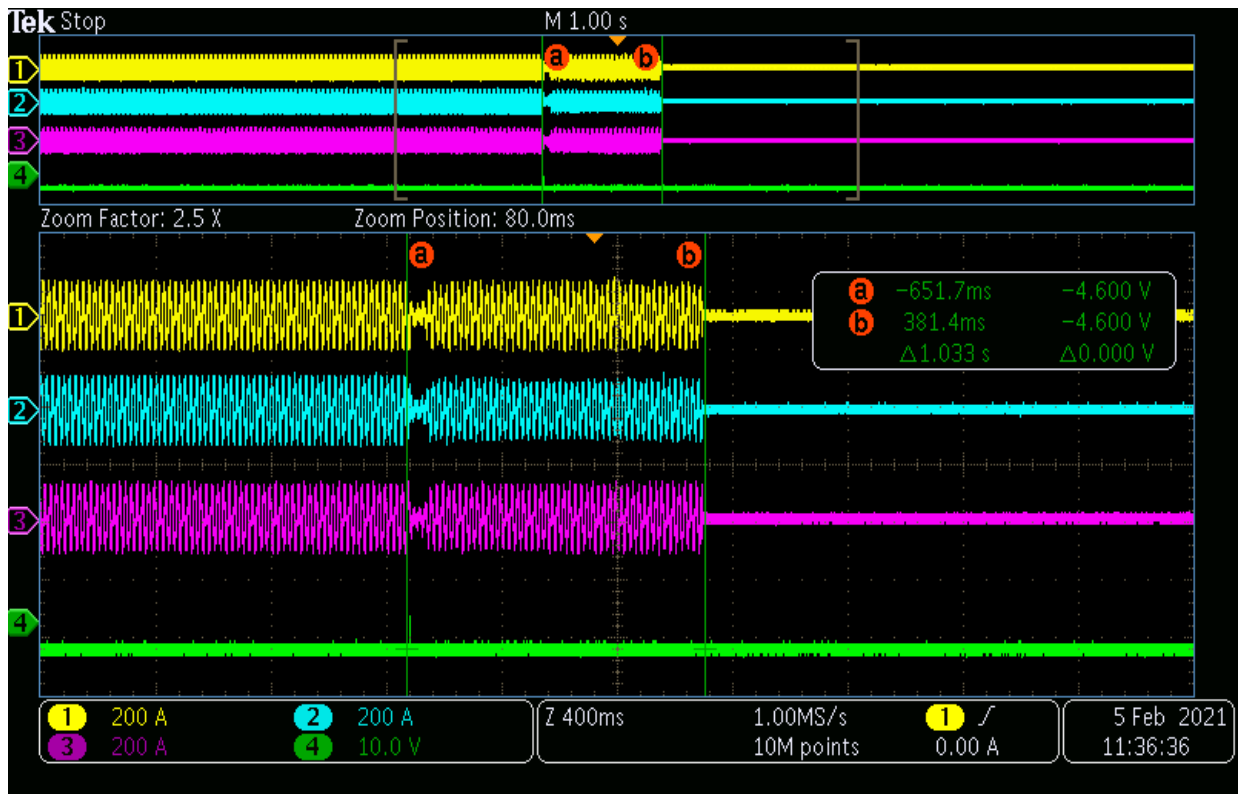
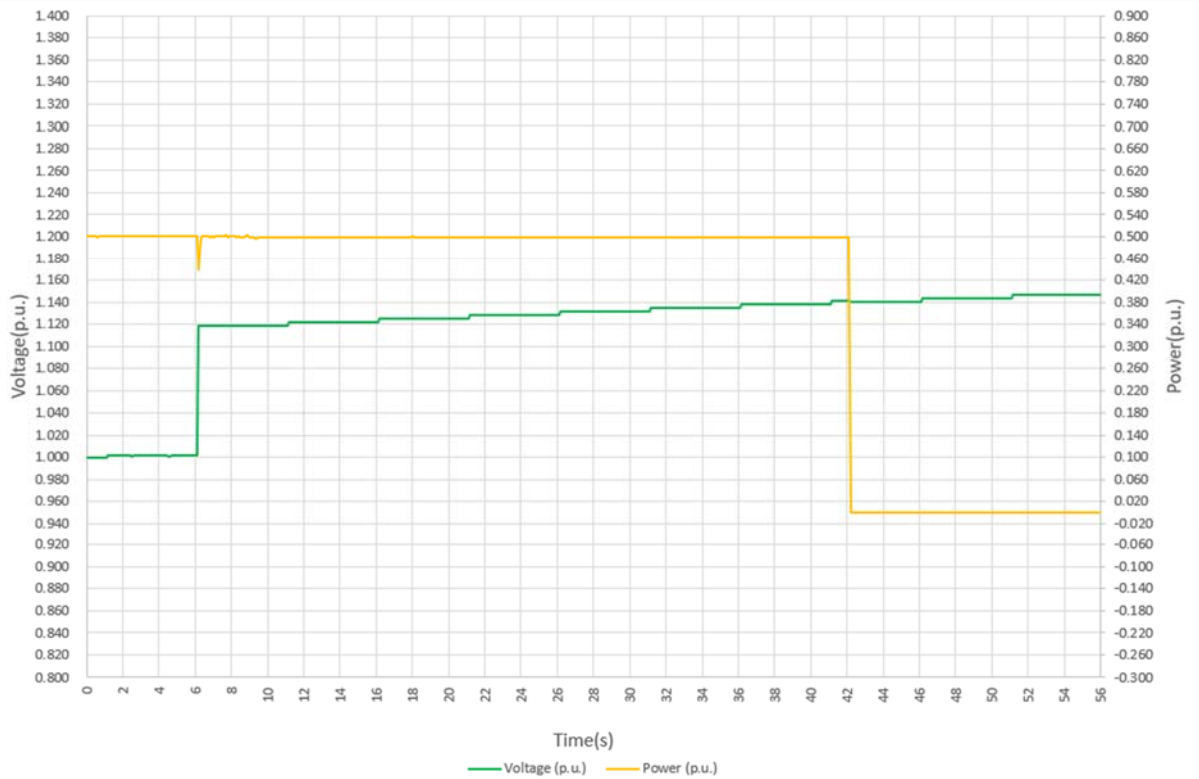
O/V stage 1-1



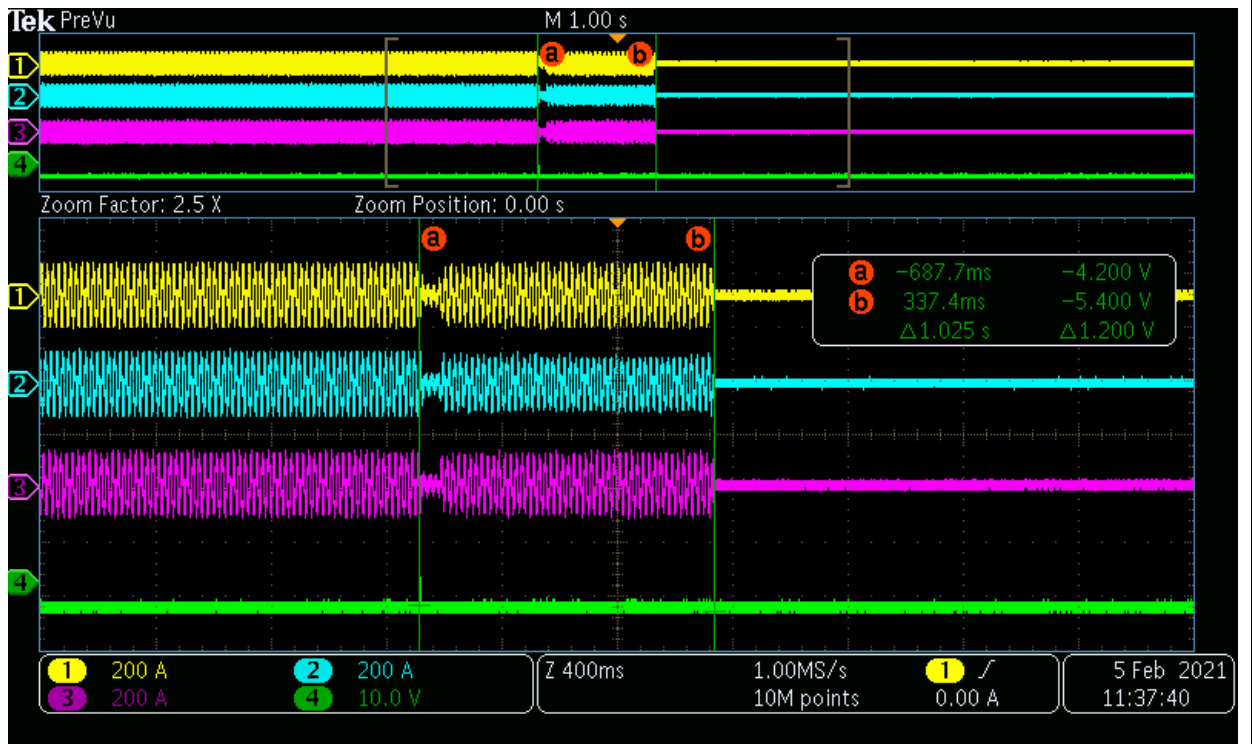
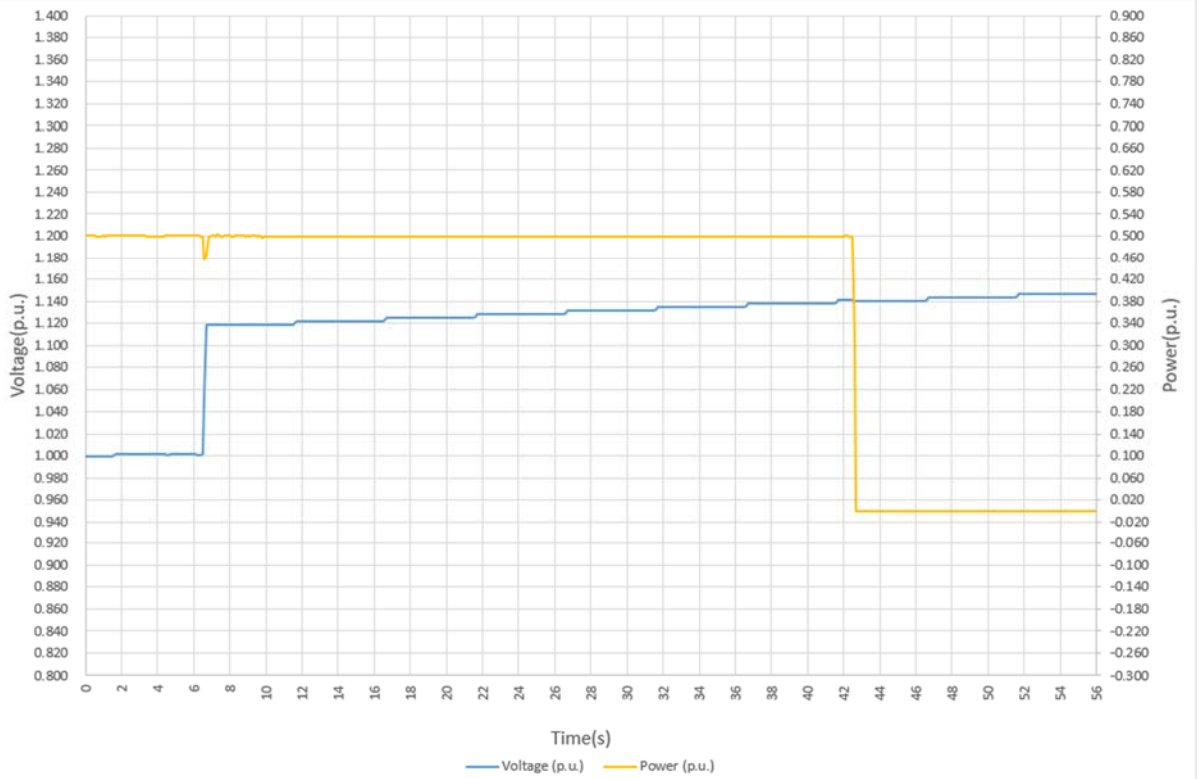
O/V stage 1-2



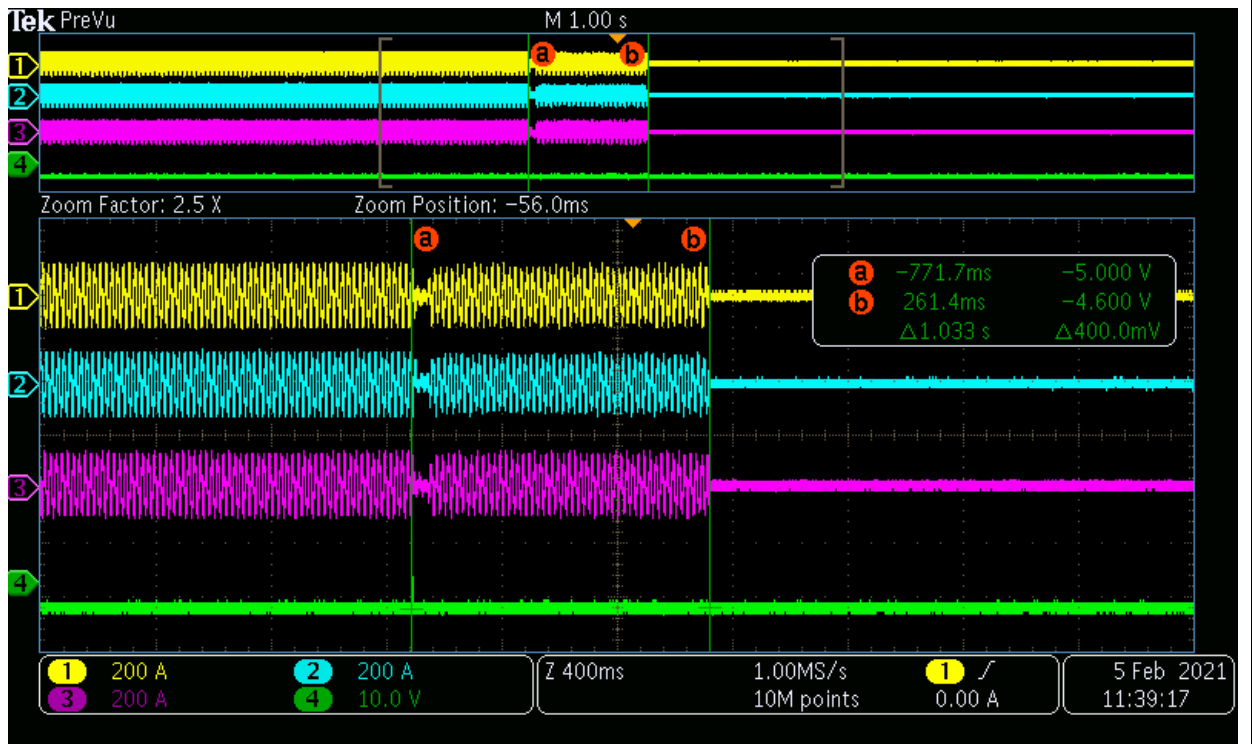
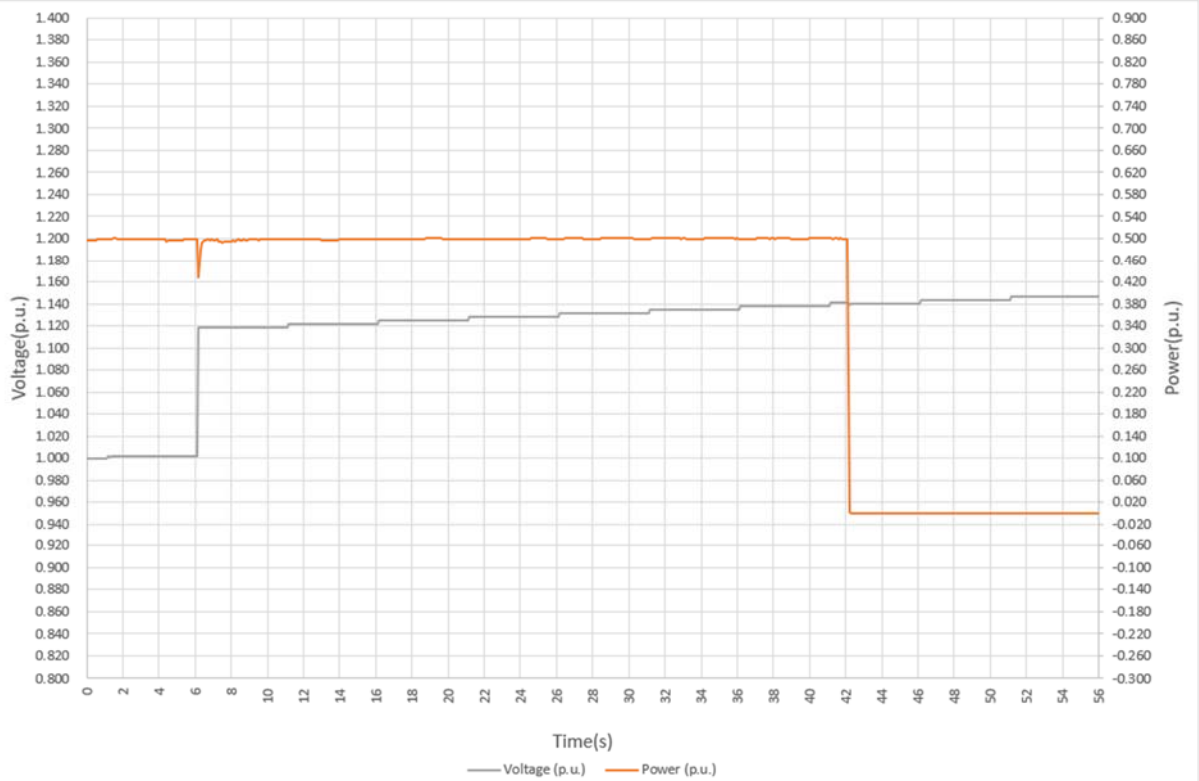
O/V stage 1-3



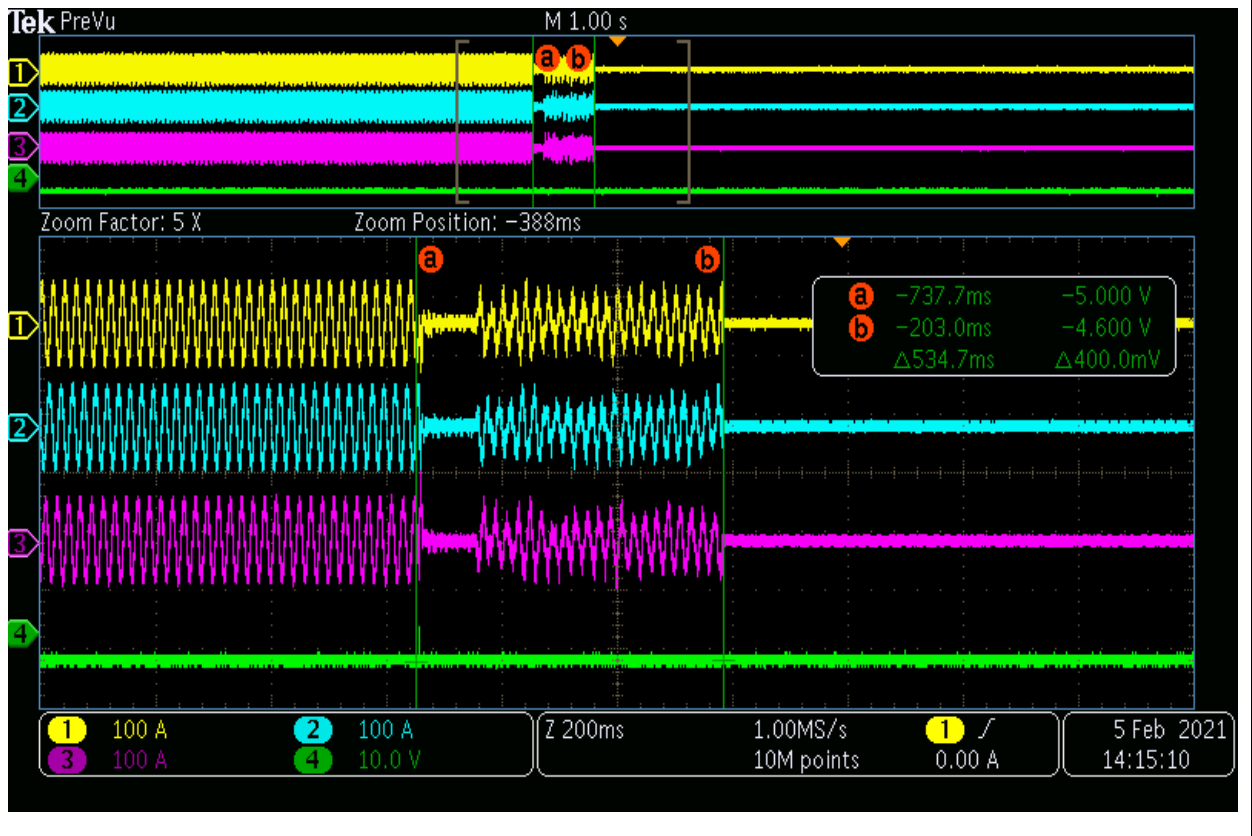
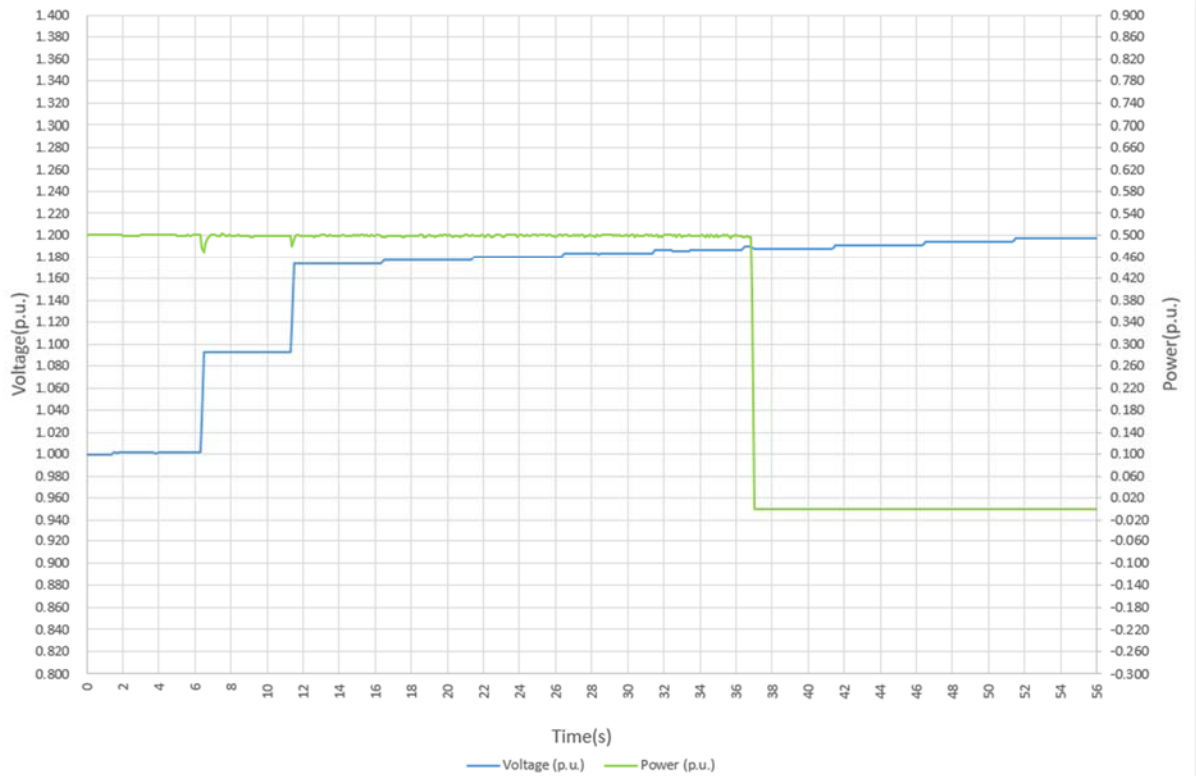
O/V stage 1-4



O/V stage 1-5

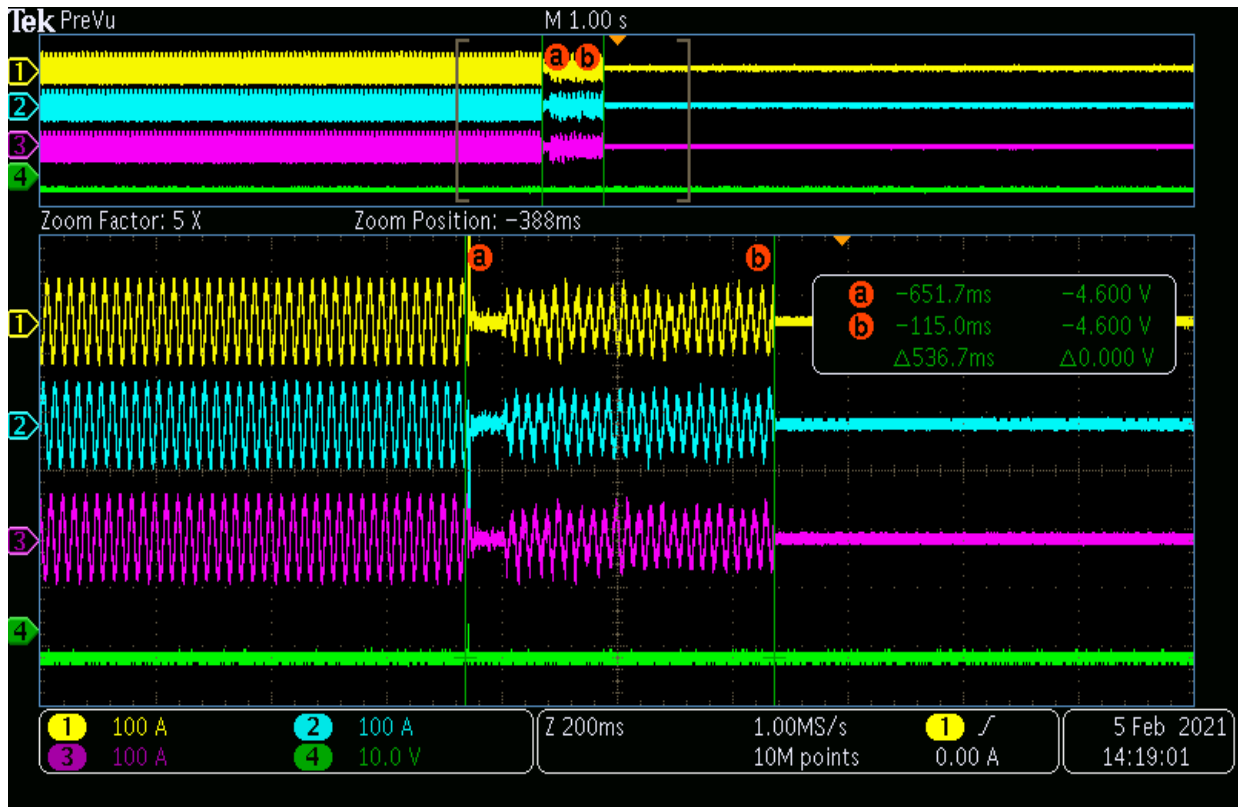
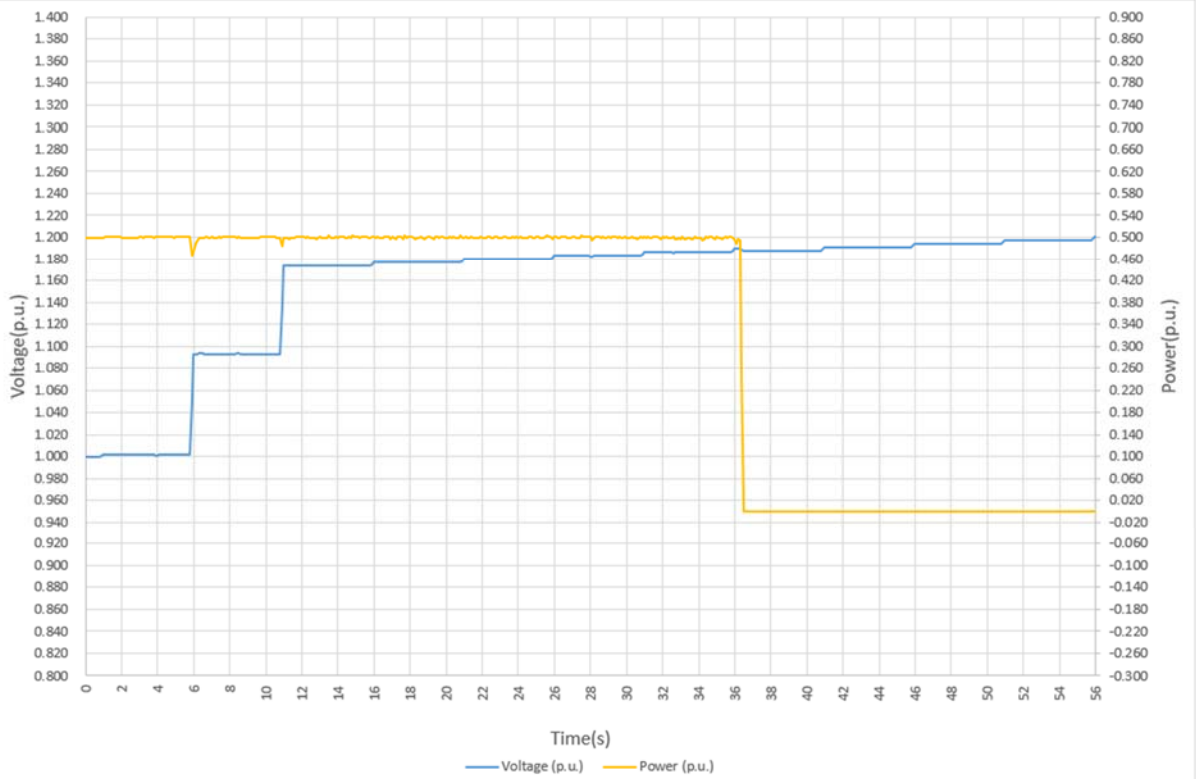


O/V stage 2-1

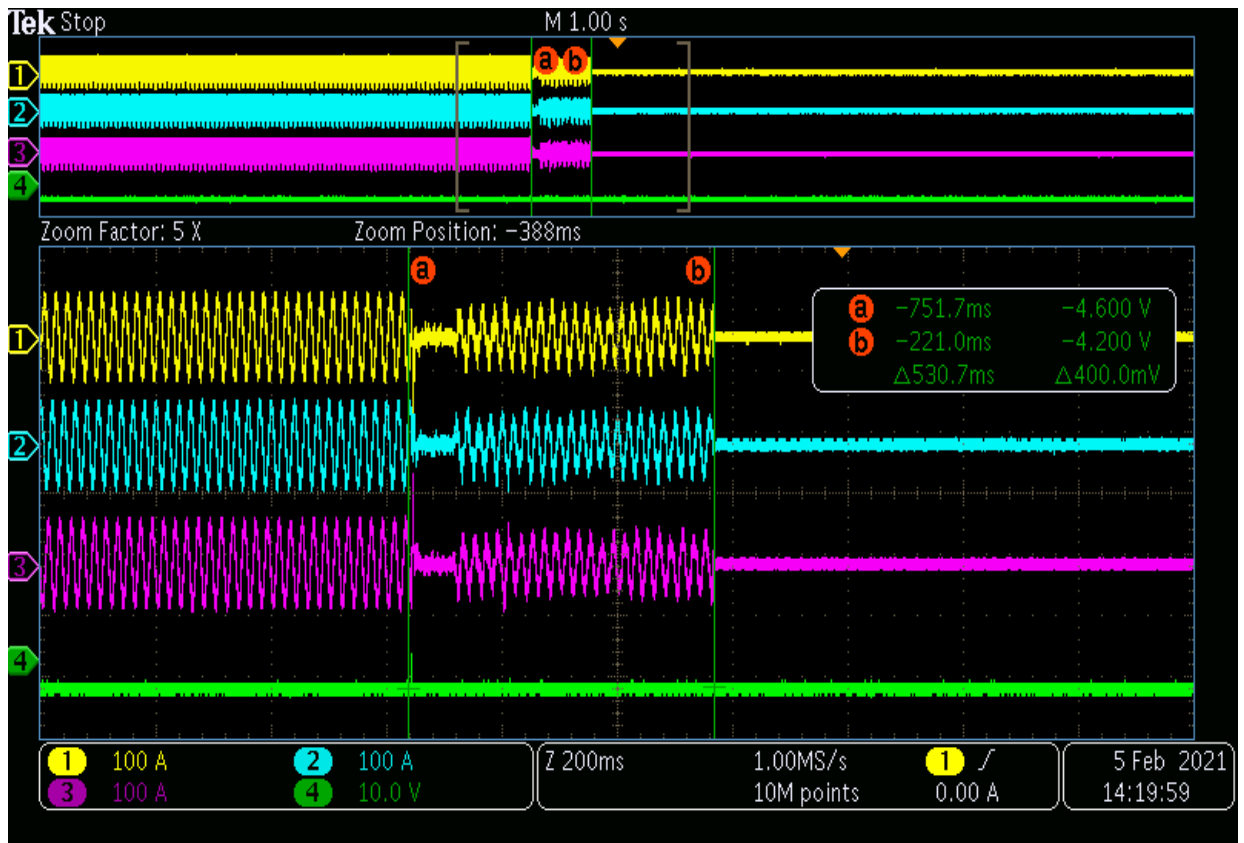
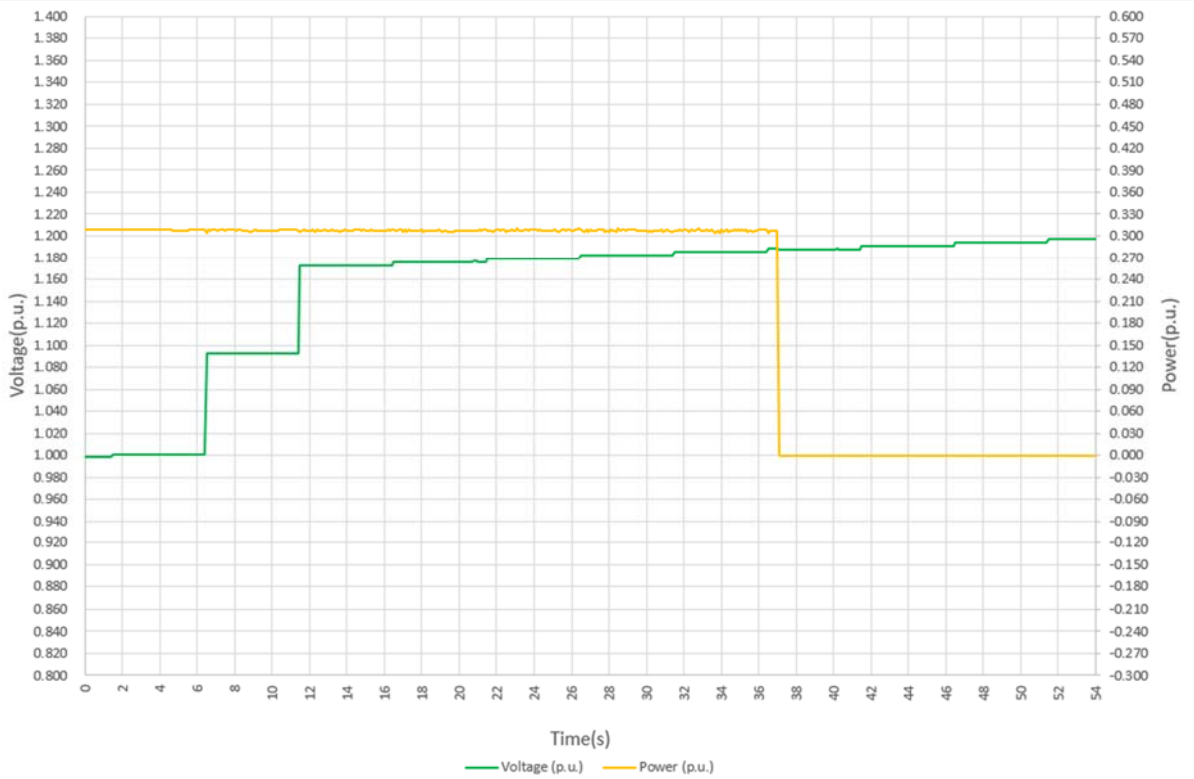




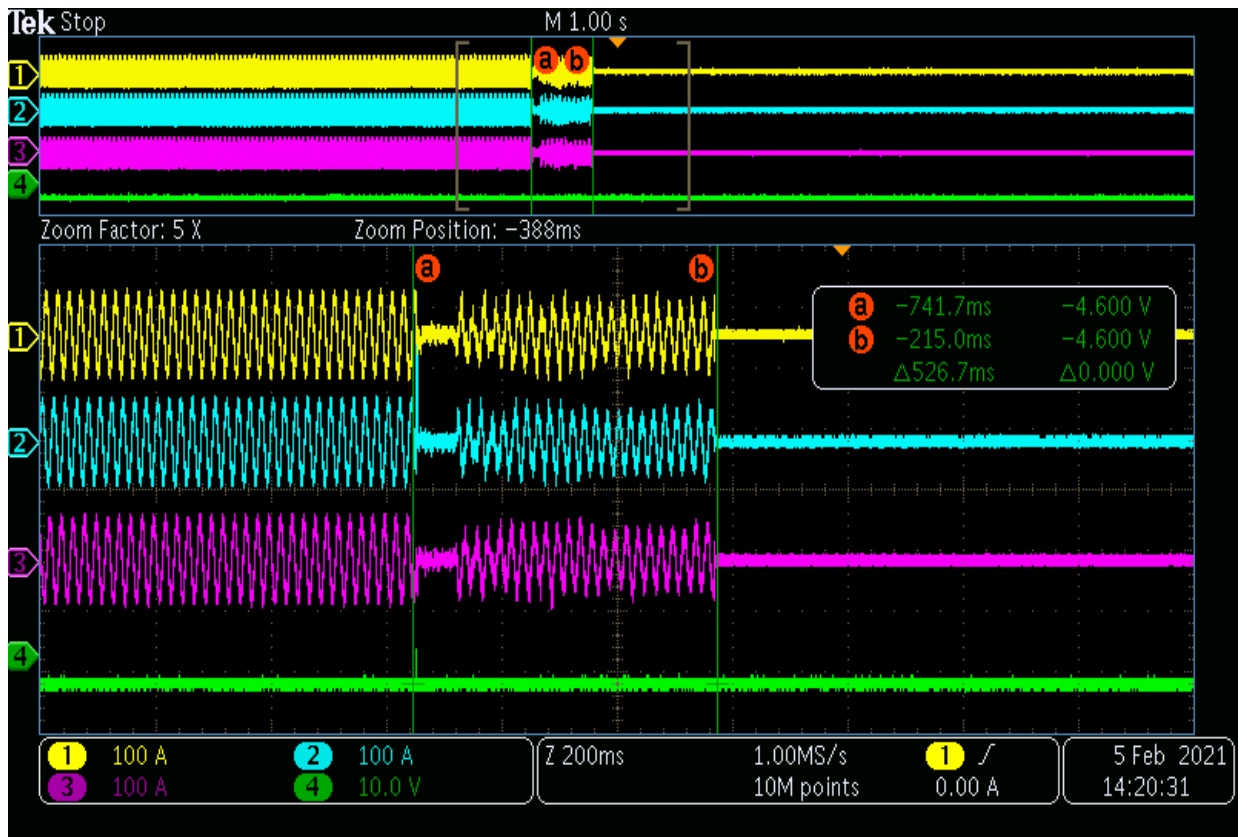
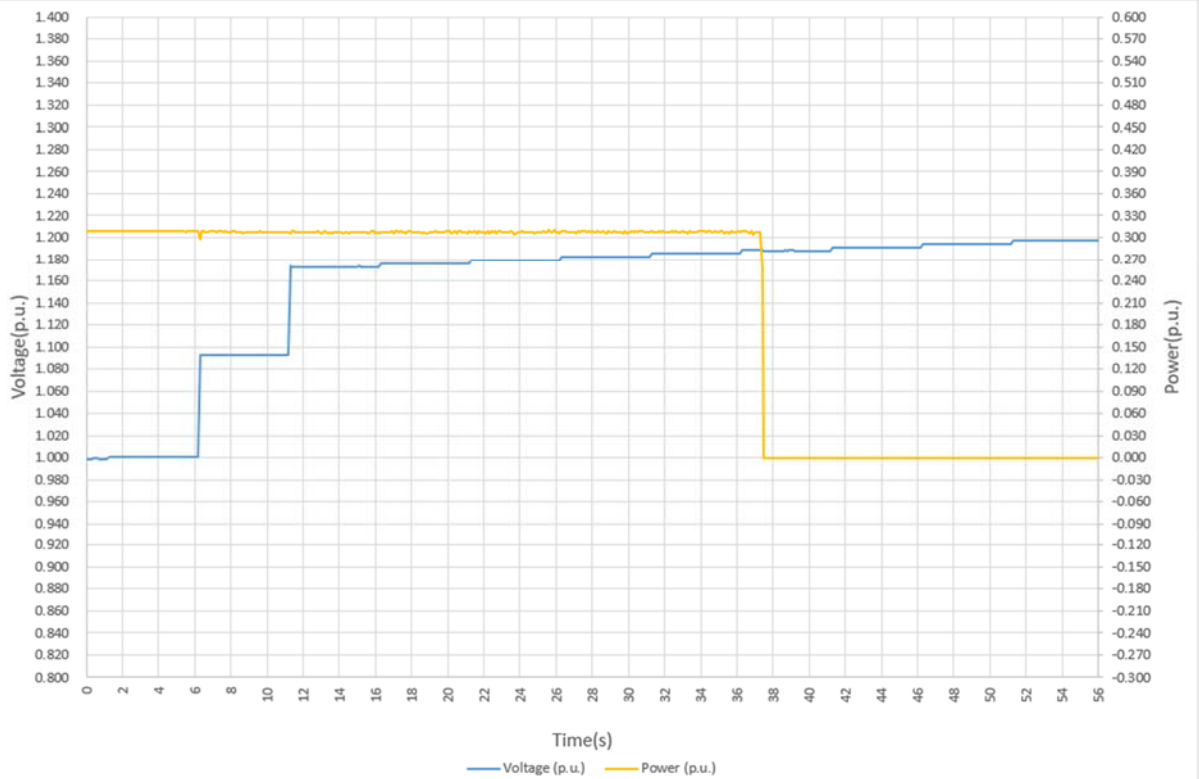
O/V stage 2-2



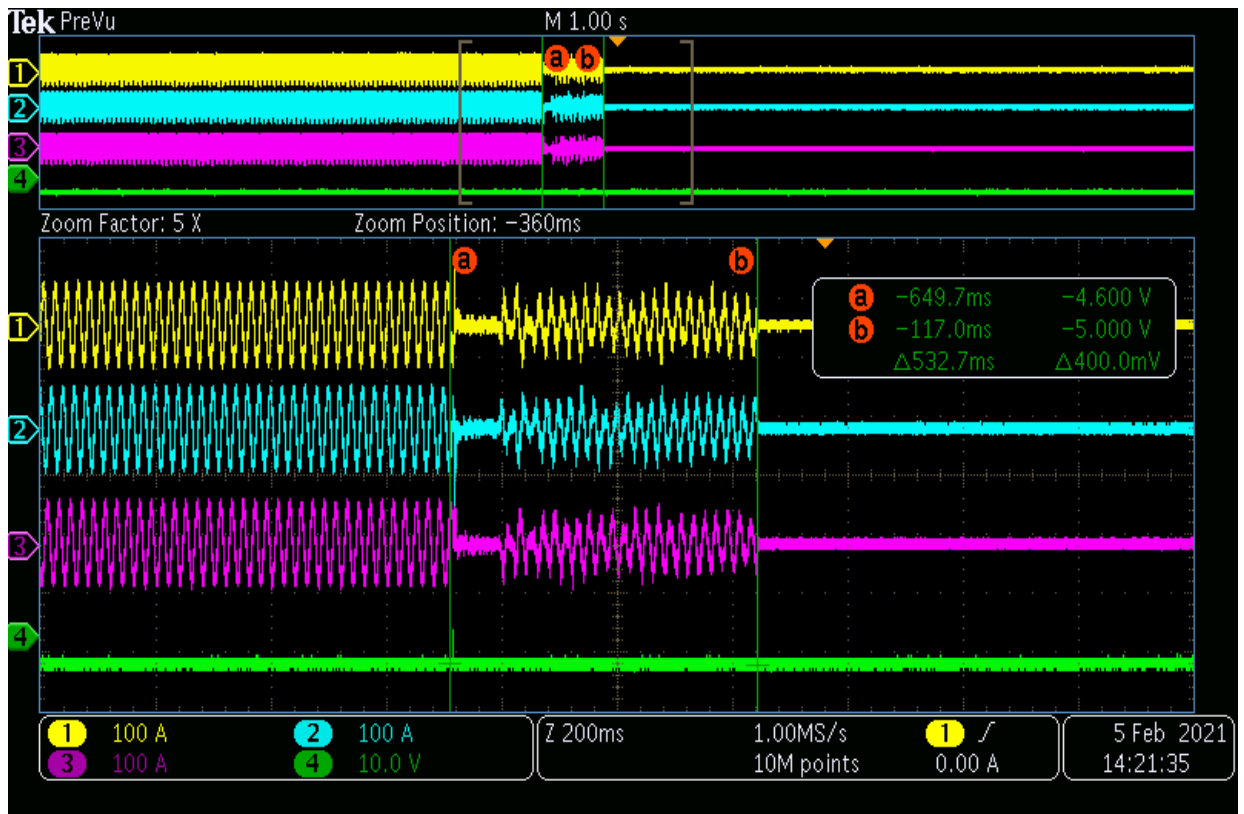
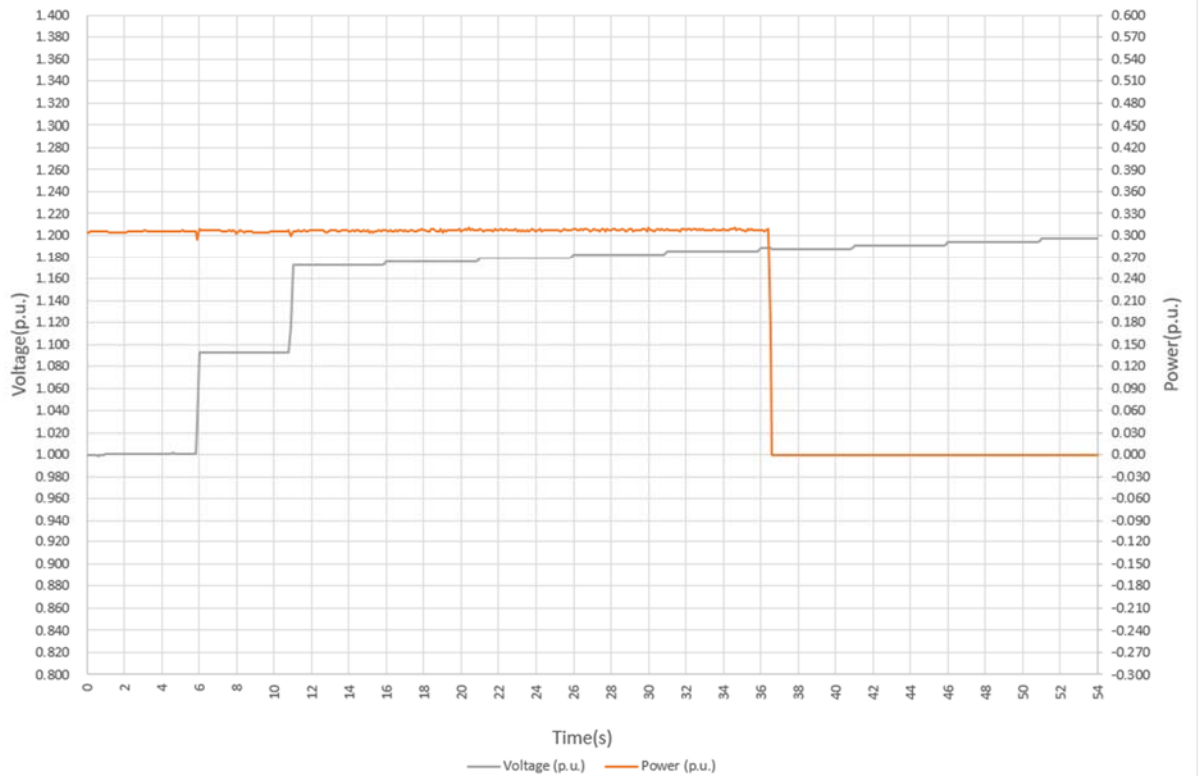
O/V stage 2-3



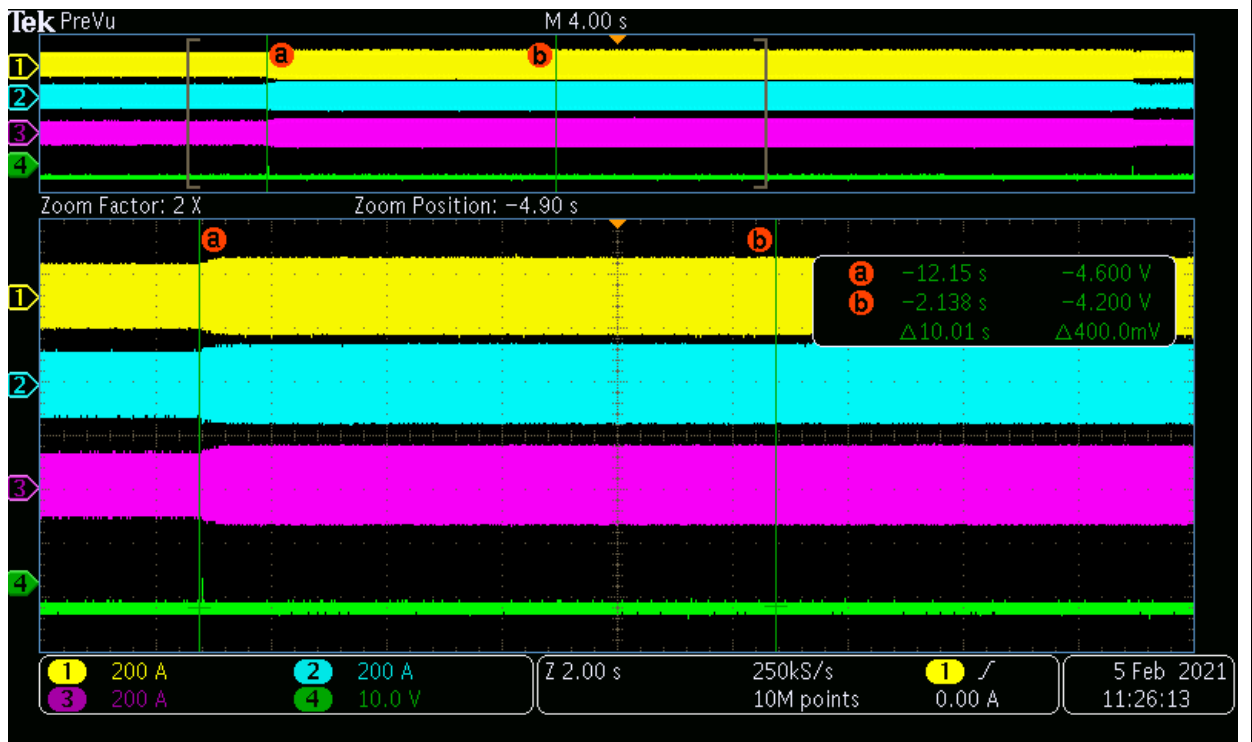
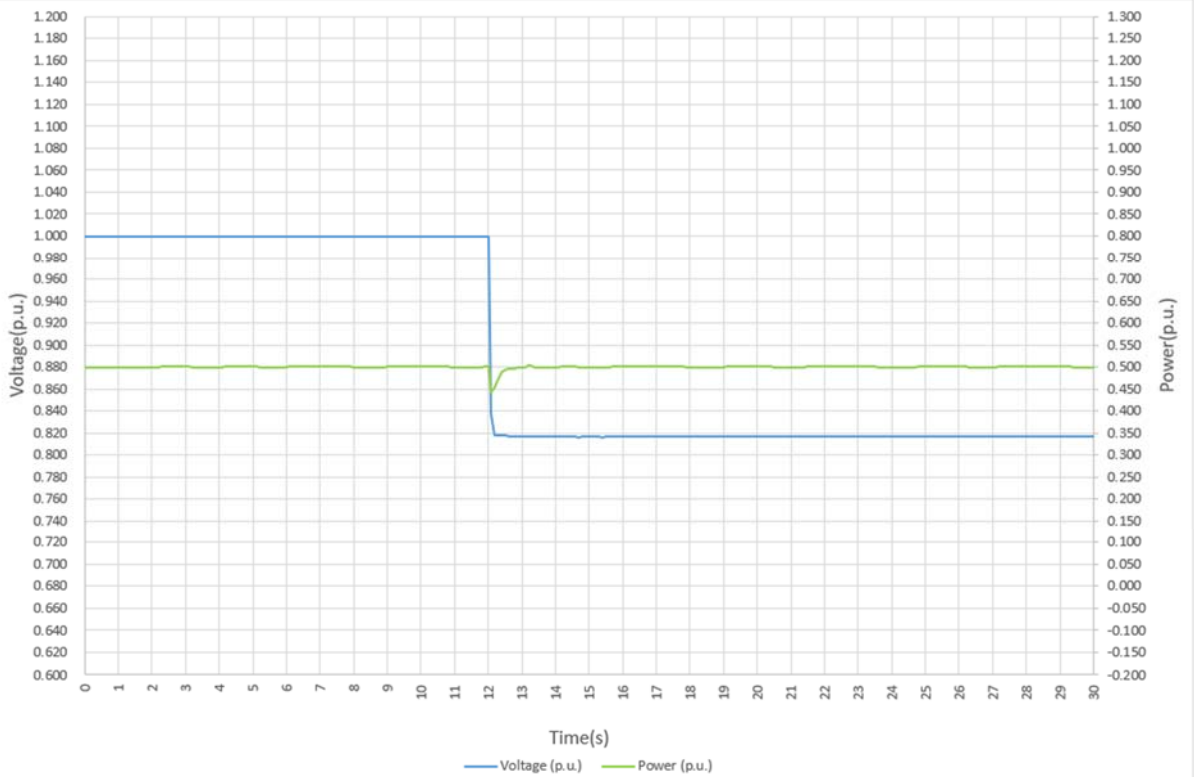
O/V stage 2-4



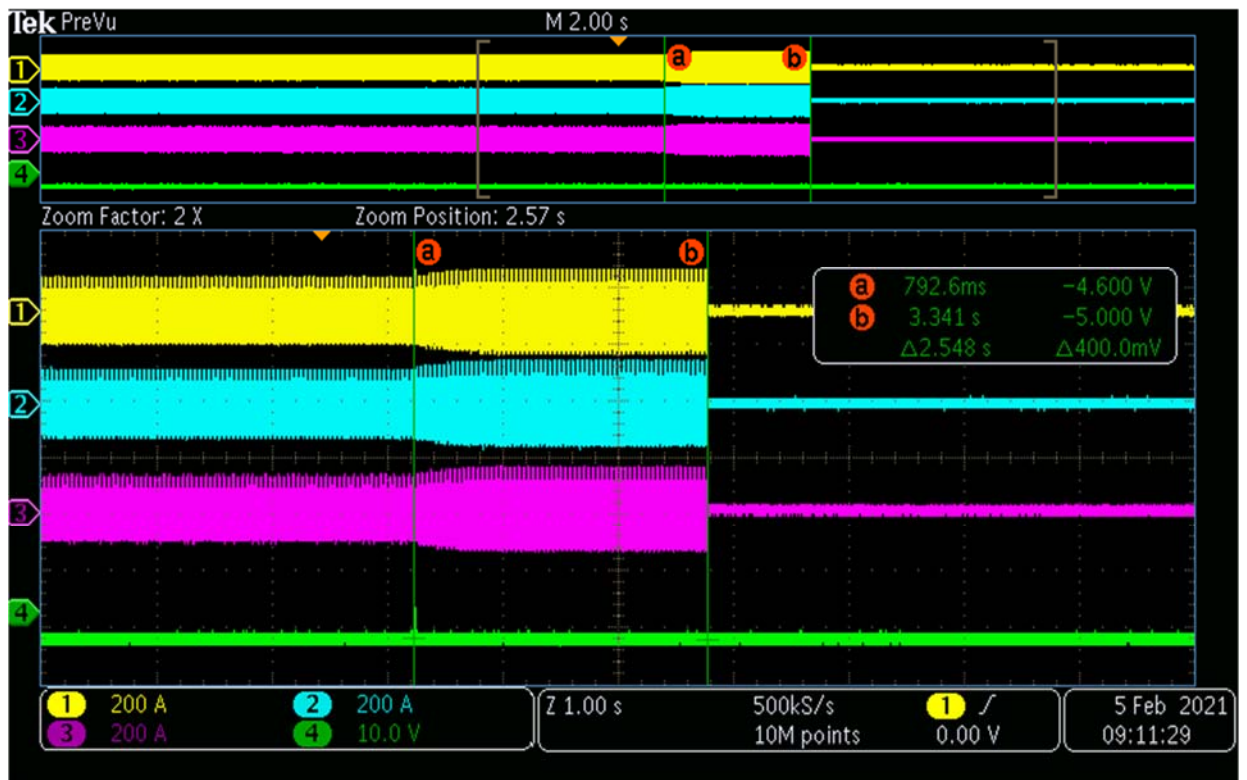
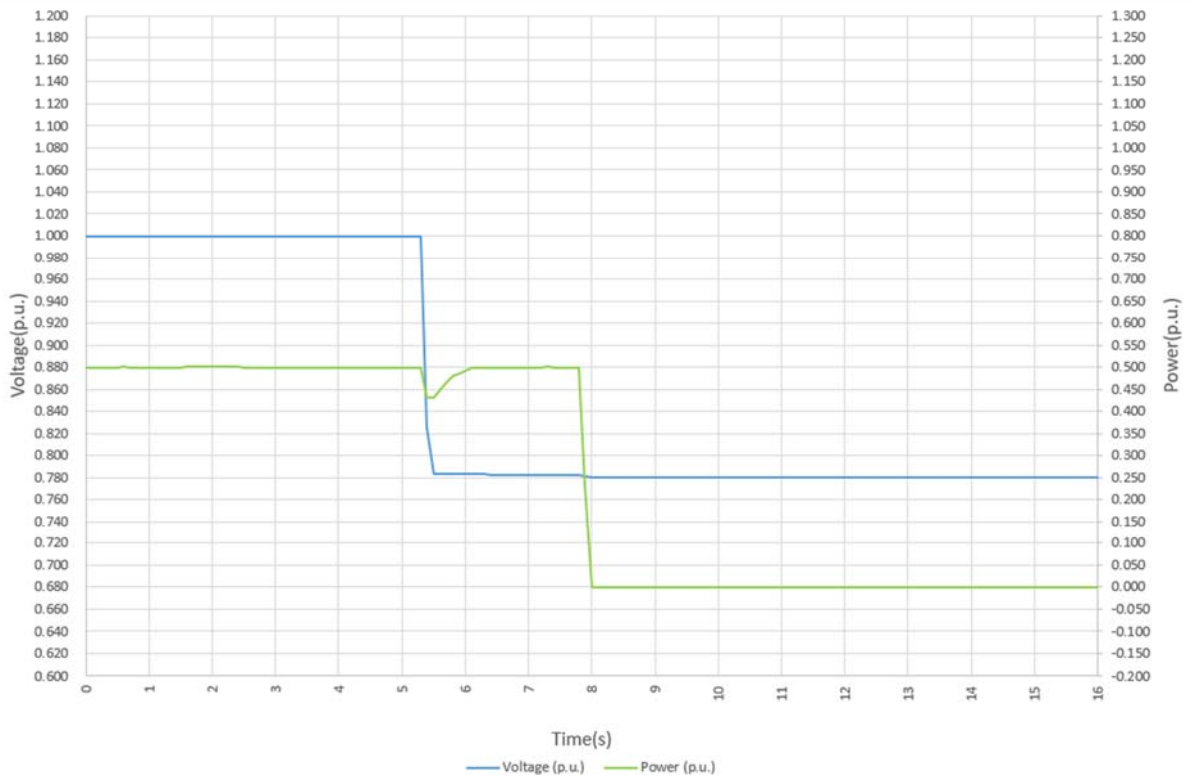
O/V stage 2-5



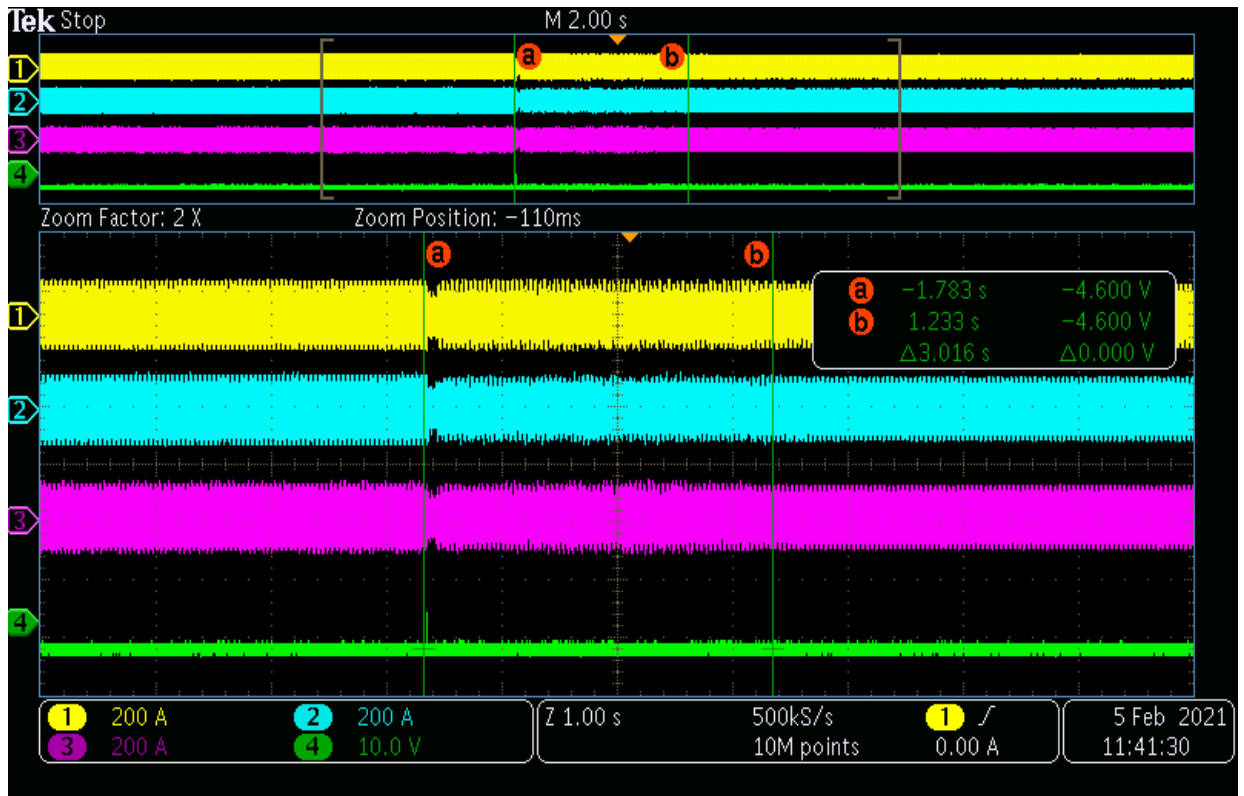
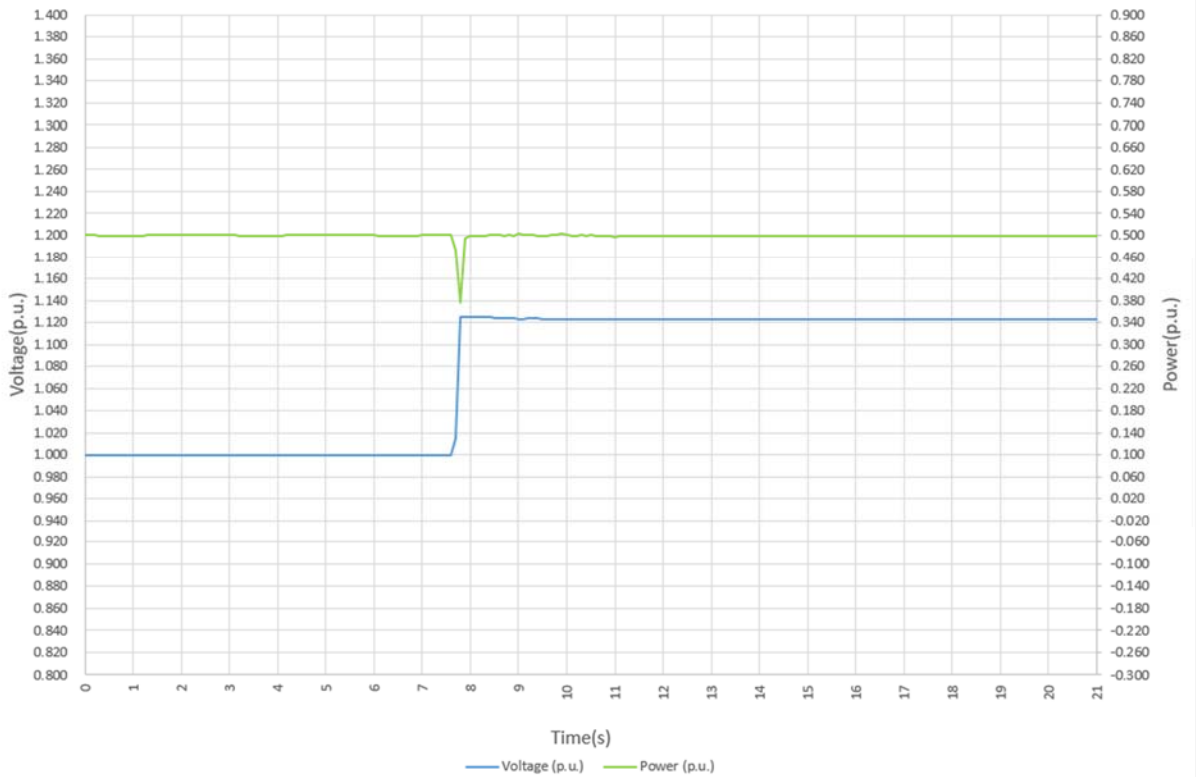
No trip tests – 254.9V



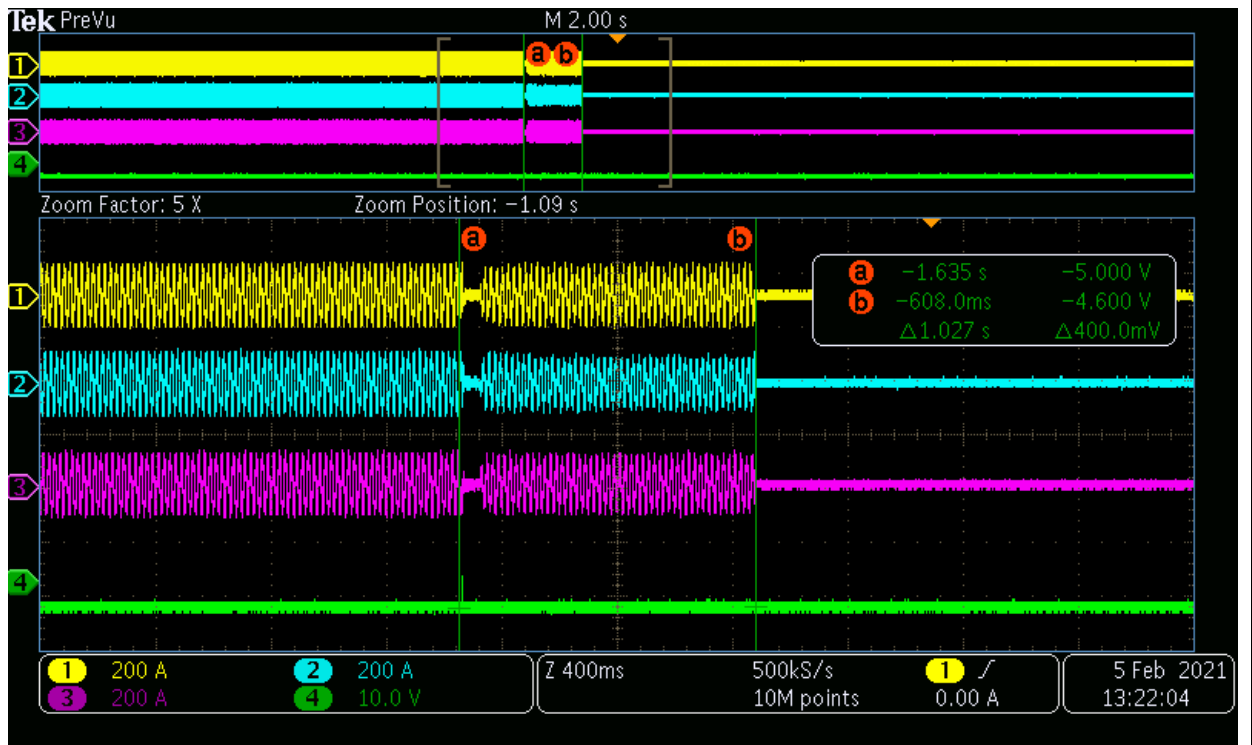
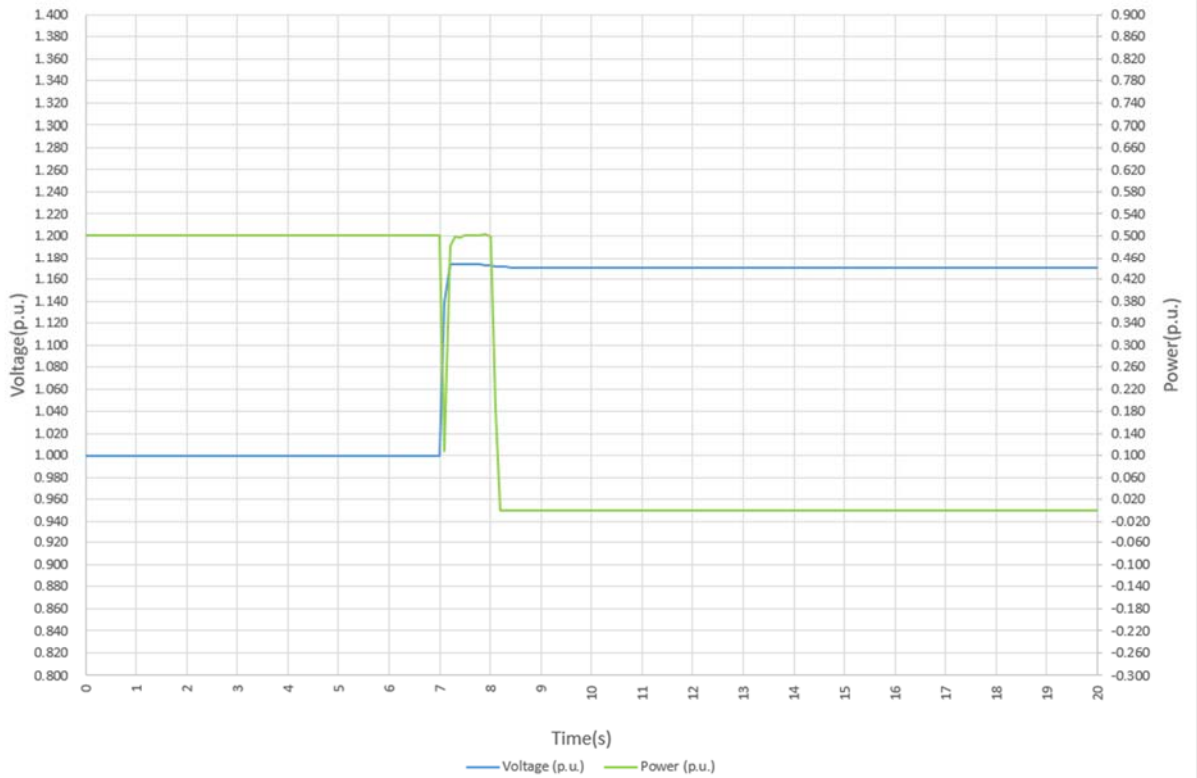
No trip tests – 244V



No trip tests – 350V

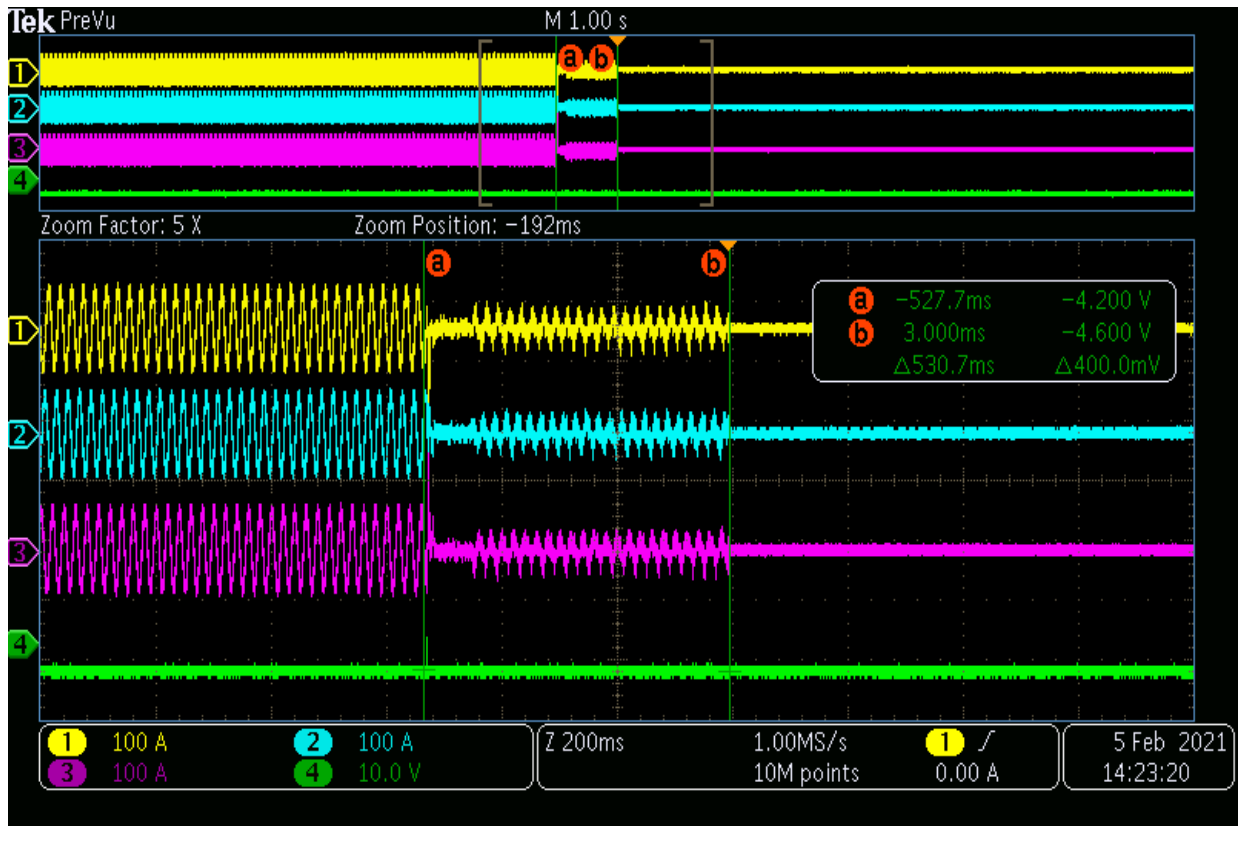
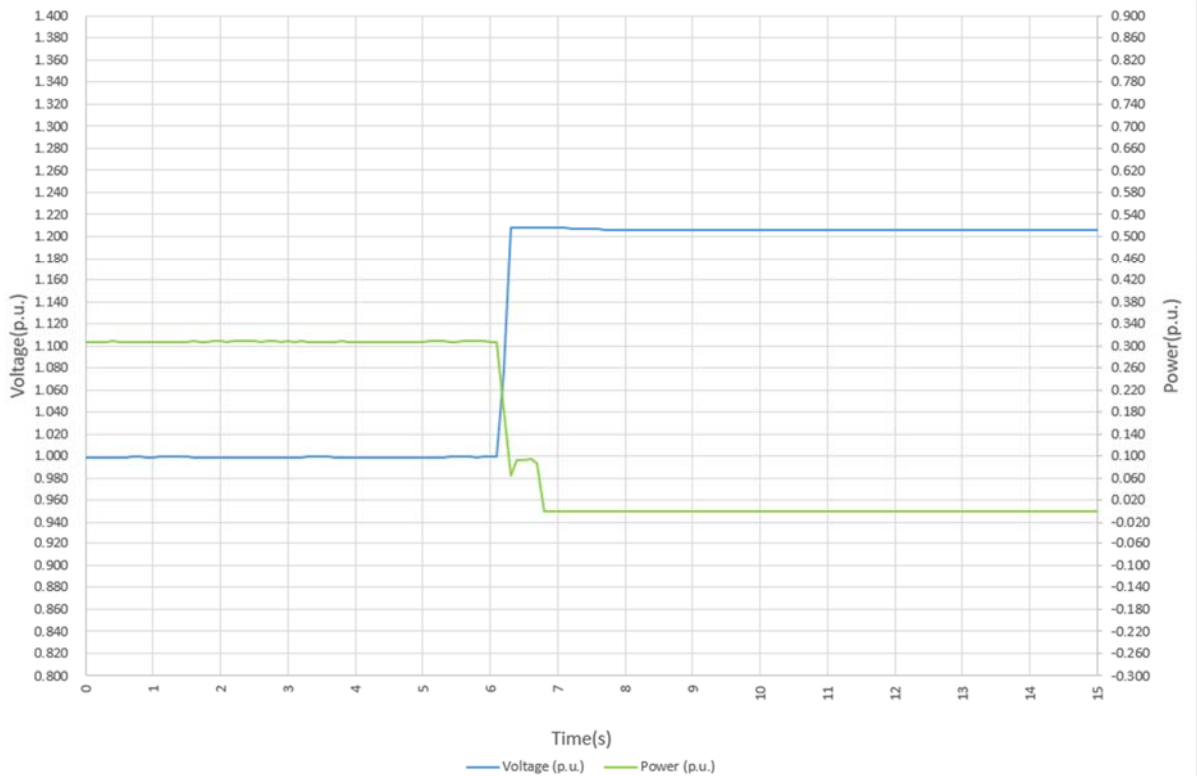


No trip tests – 365.6V





No trip tests -376.5V



#### 4.3.3 Loss of Mains test

These tests should be carried out in accordance with BS EN 62116. Annex A.7.1.2.4.

The maximum trip time is 0.5 s.

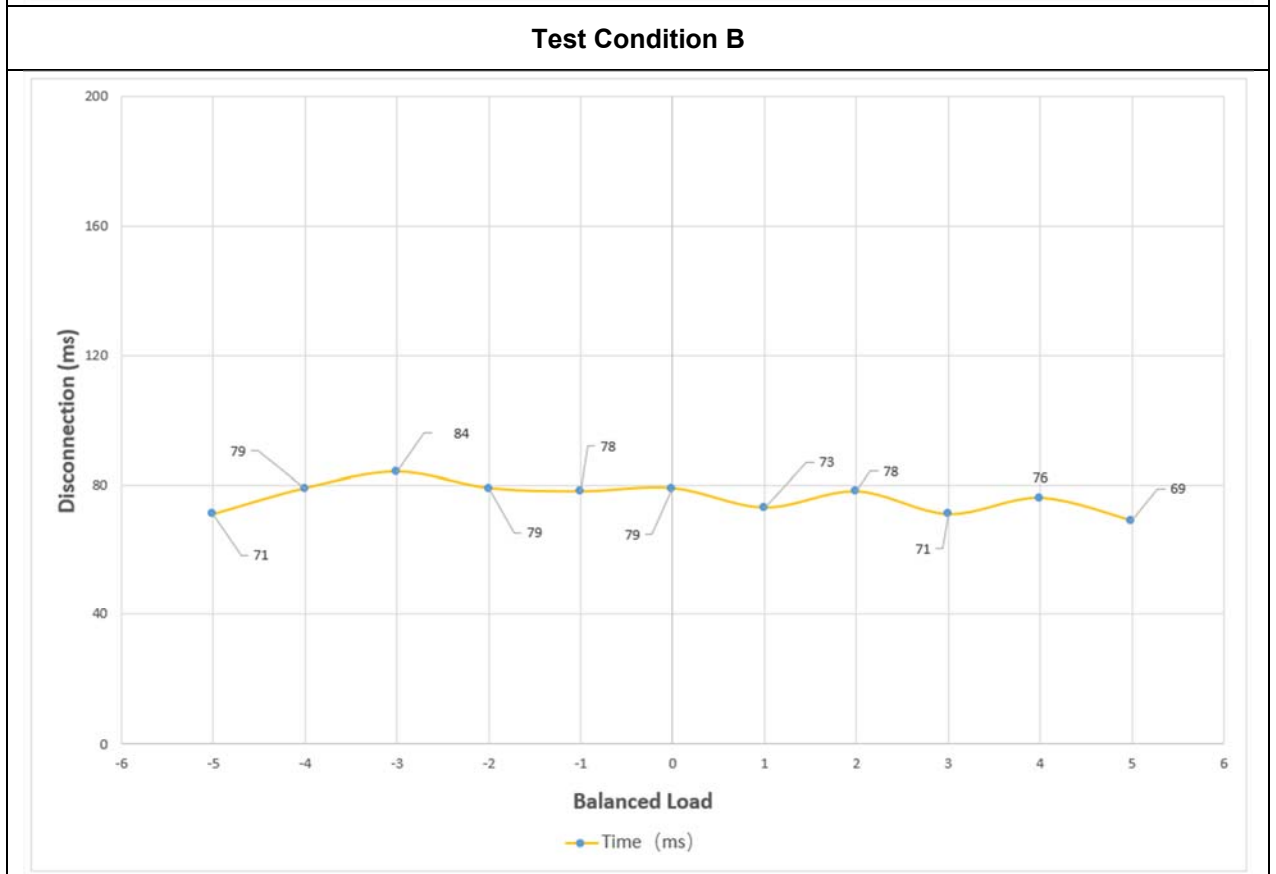
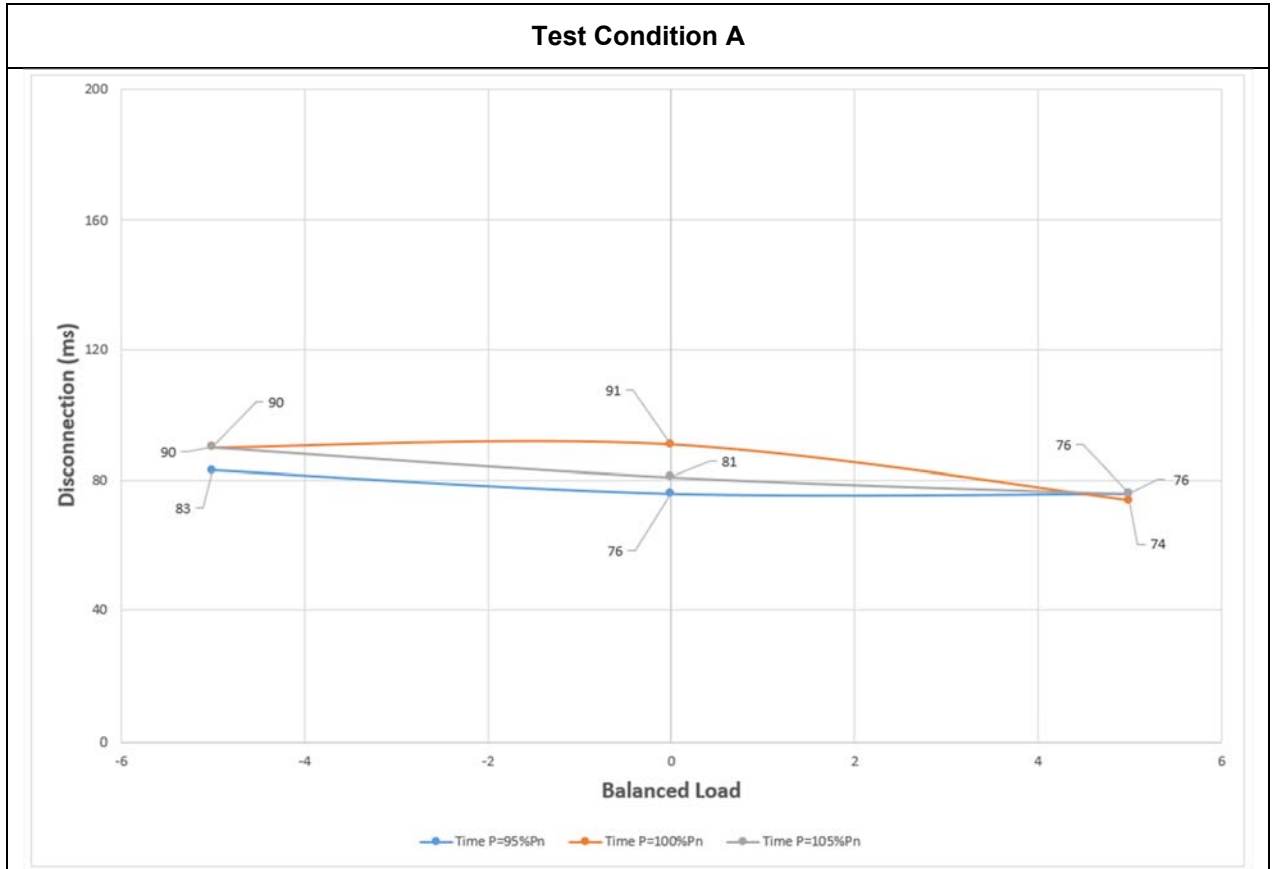
Note for technologies which have a substantial shut down time this can be added to the 0.5 s in establishing that the trip occurred in less than 0.5 s. Maximum shut down time could therefore be up to 1.0 s for these technologies.

Following tables show the test results:

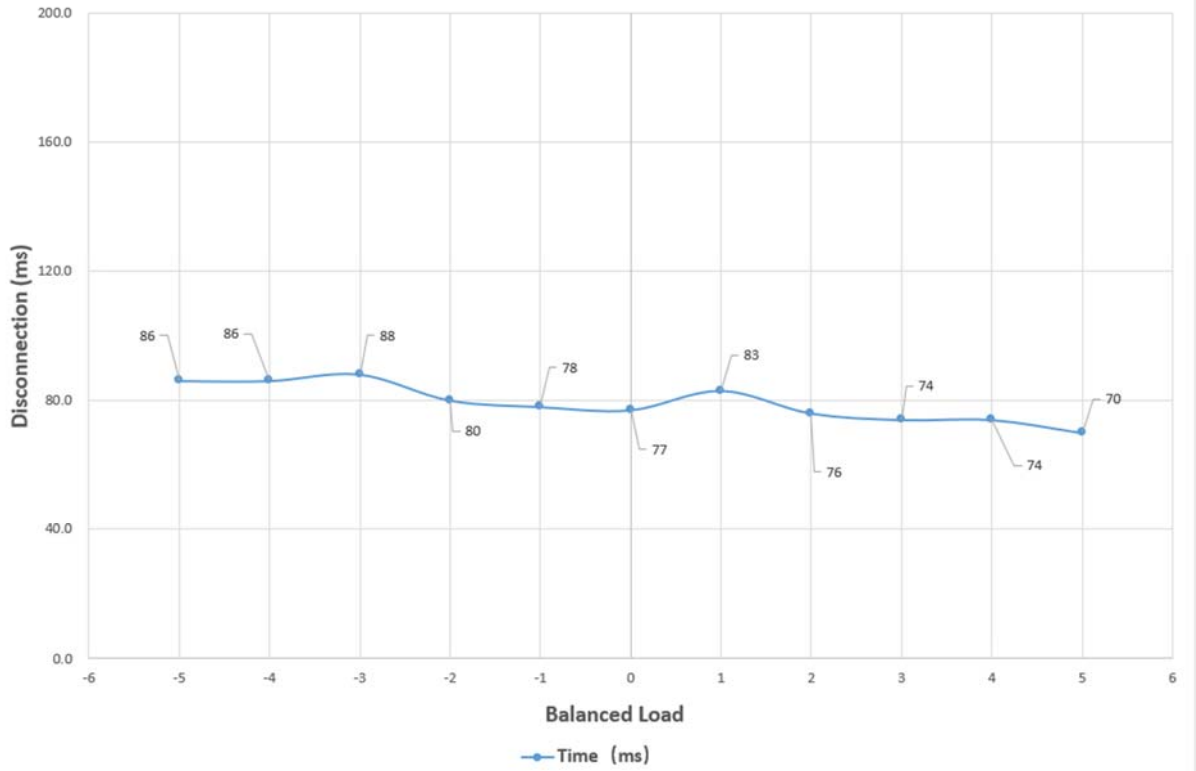
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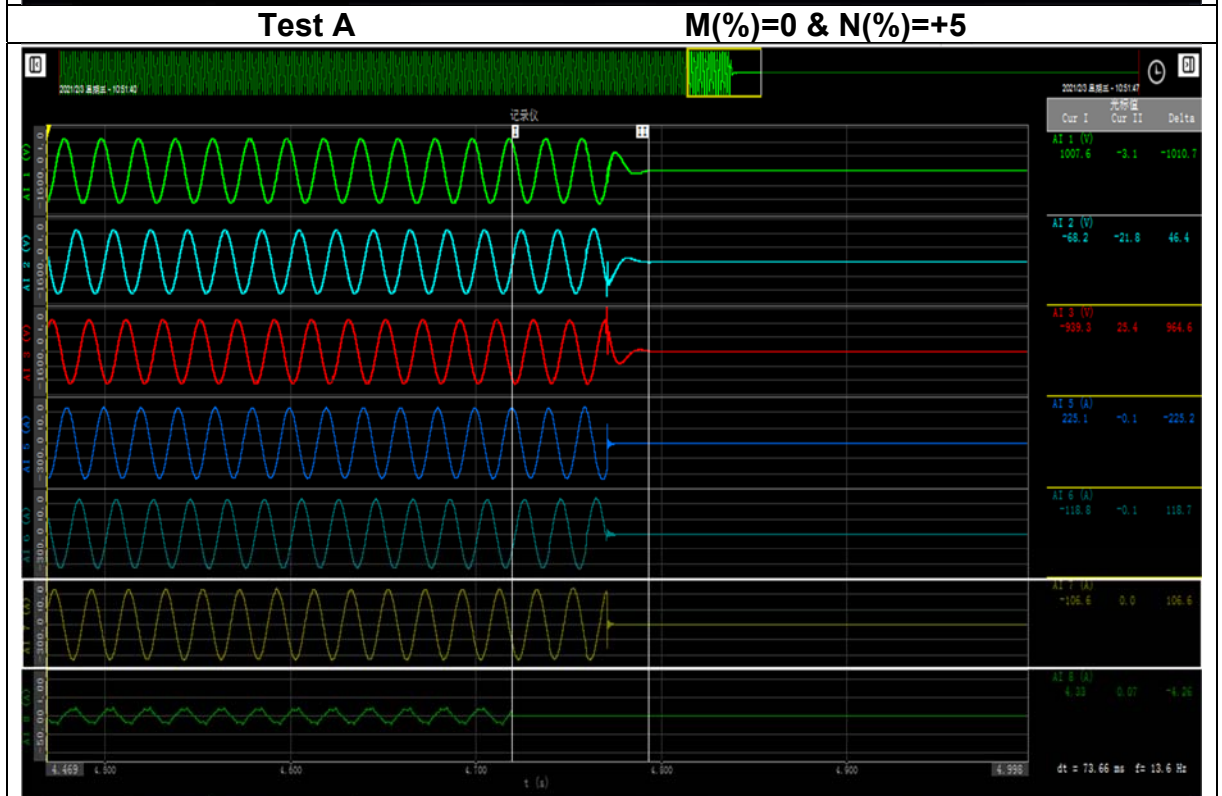
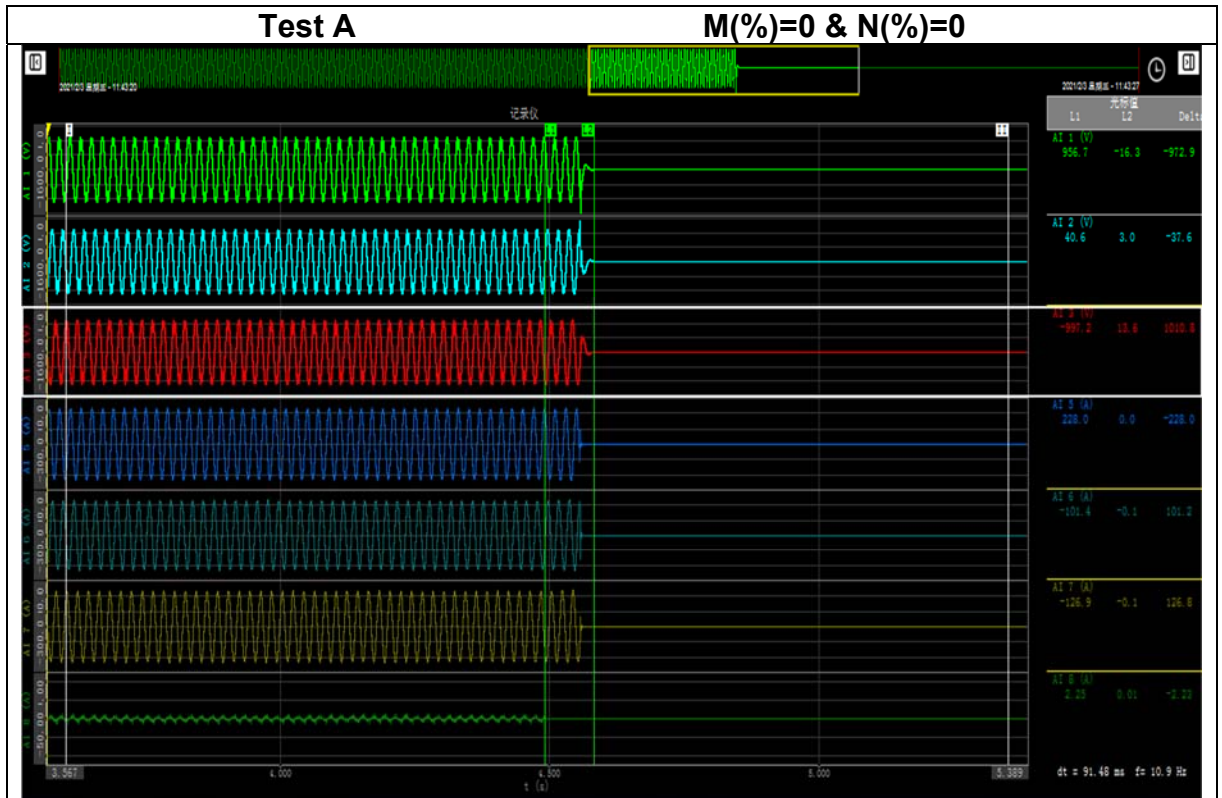
Table: tested condition and trip time						P
No.	P <sub>EUT</sub> (% of EUT rating)	Reactive load (% of normal)	P <sub>AC</sub>	Q <sub>AC</sub>	Trip time(s)	Which load is selected to be adjusted (R or L)
Test condition A						
1	100	100	0	0	91	--
2	100	100	-5	-5	83	R/L
3	100	100	-5	0	76	R
4	100	100	-5	+5	76	R/L
5	100	100	0	-5	90	L
6	100	100	0	+5	74	L
7	100	100	+5	-5	90	R/L
8	100	100	+5	0	81	R
9	100	100	+5	+5	76	R/L
10	100	100	-10	+10	--	R/L
11	100	100	-5	+10	--	R/L
12	100	100	0	+10	--	L
13	100	100	+10	+10	--	R/L
14	100	100	+10	+5	--	R/L
15	100	100	+10	0	--	R
16	100	100	+10	-5	--	R/L
17	100	100	+10	-10	--	R/L
18	100	100	+5	-10	--	R/L
19	100	100	+5	+10	--	R/L
20	100	100	0	-10	--	L
21	100	100	-5	-10	--	R/L
22	100	100	-10	-10	--	R/L
23	100	100	-10	-5	--	R/L
24	100	100	-10	0	--	R
25	100	100	-10	+5	--	R/L
Test condition B						
1	66	66	0	0	79	--
2	66	66	0	71	353	L
3	66	66	0	79	452	L
4	66	66	0	84	395	L
5	66	66	0	79	328	L
6	66	66	0	78	389	L
7	66	66	0	73	466	L
8	66	66	0	78	391	L
9	66	66	0	71	364	L
10	66	66	0	76	345	L
11	66	66	0	69	329	L
Test condition C						
1	33	33	0	0	77	--
2	33	33	0	-5	86	L
3	33	33	0	-4	86	L
4	33	33	0	-3	88	L
5	33	33	0	-2	80	L
6	33	33	0	-1	78	L
7	33	33	0	1	83	L
8	33	33	0	2	76	L
9	33	33	0	3	74	L
10	33	33	0	4	74	L
11	33	33	0	5	70	L

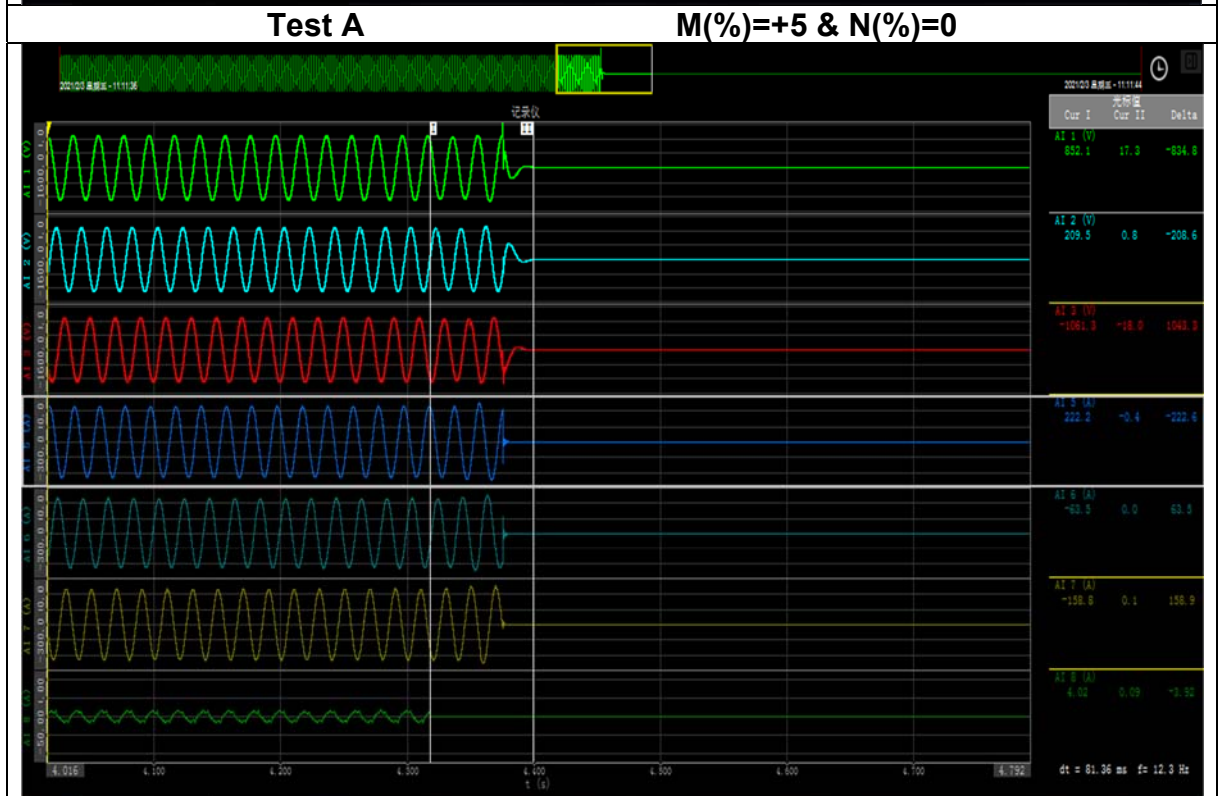
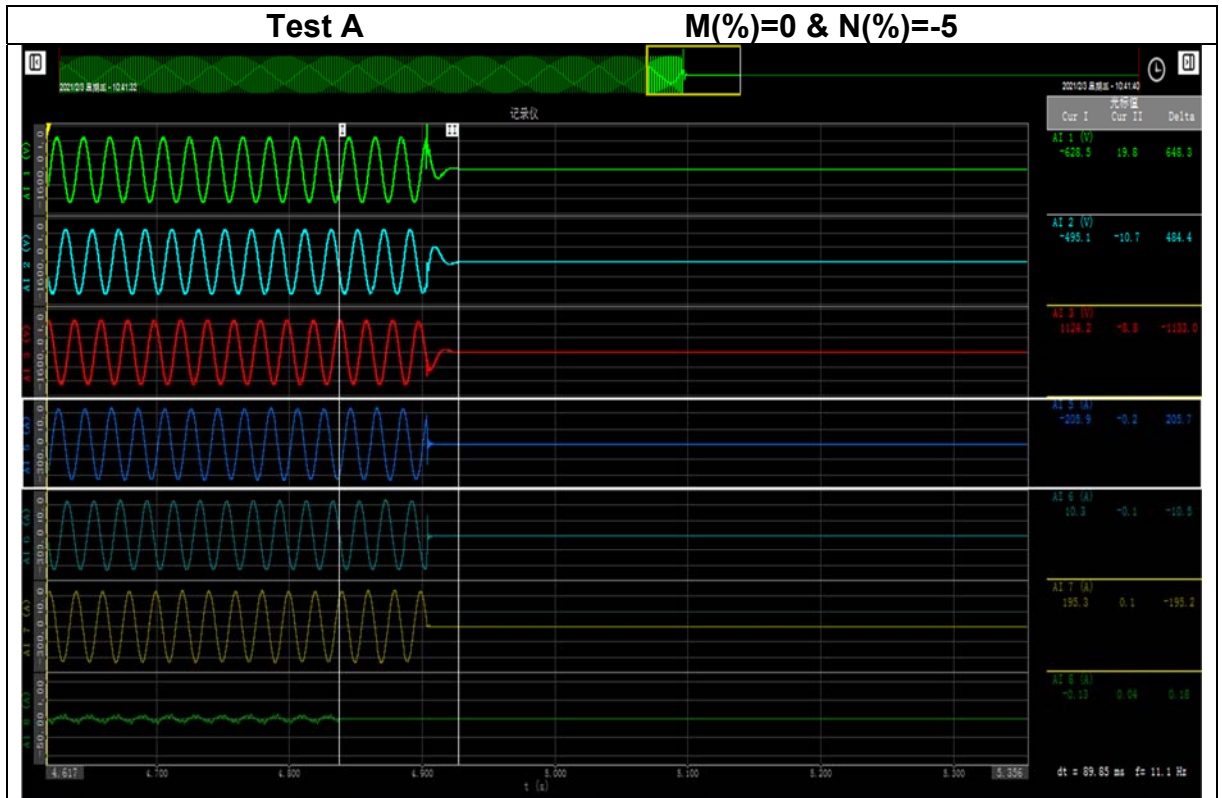
Test results are graphically shown in following pages.

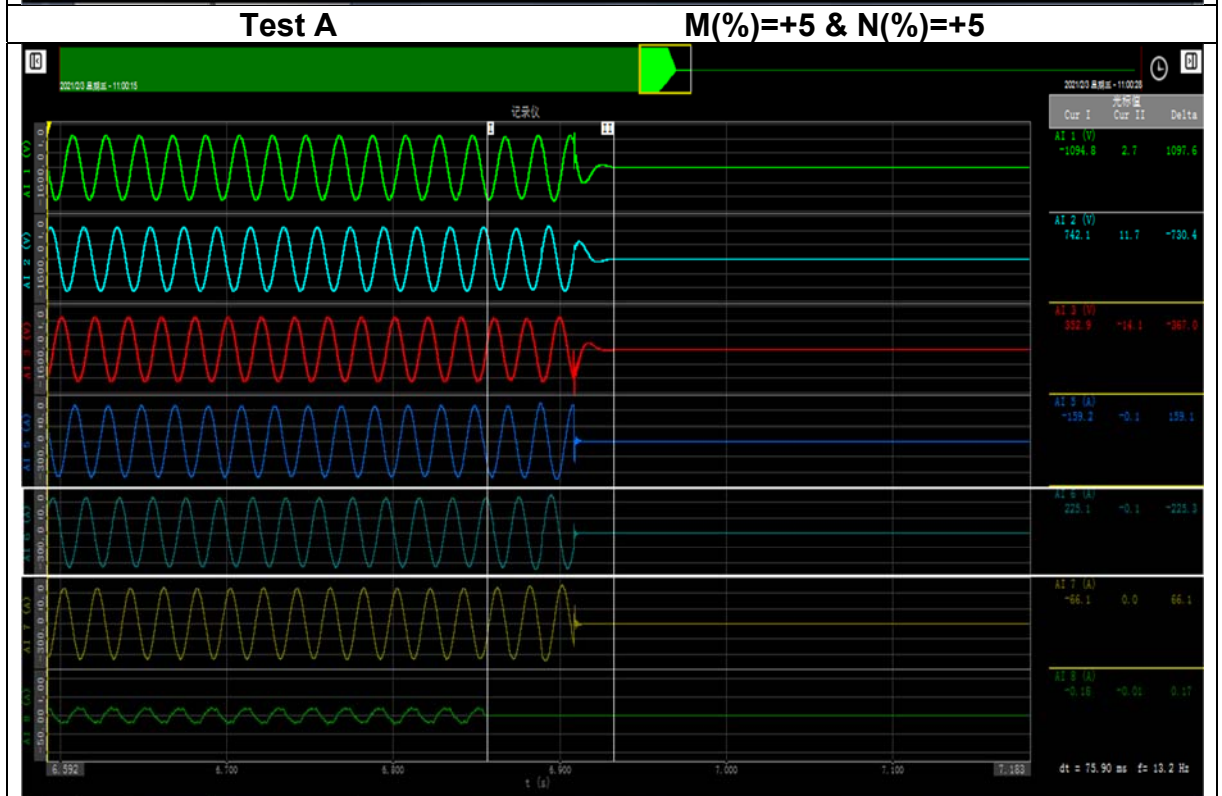
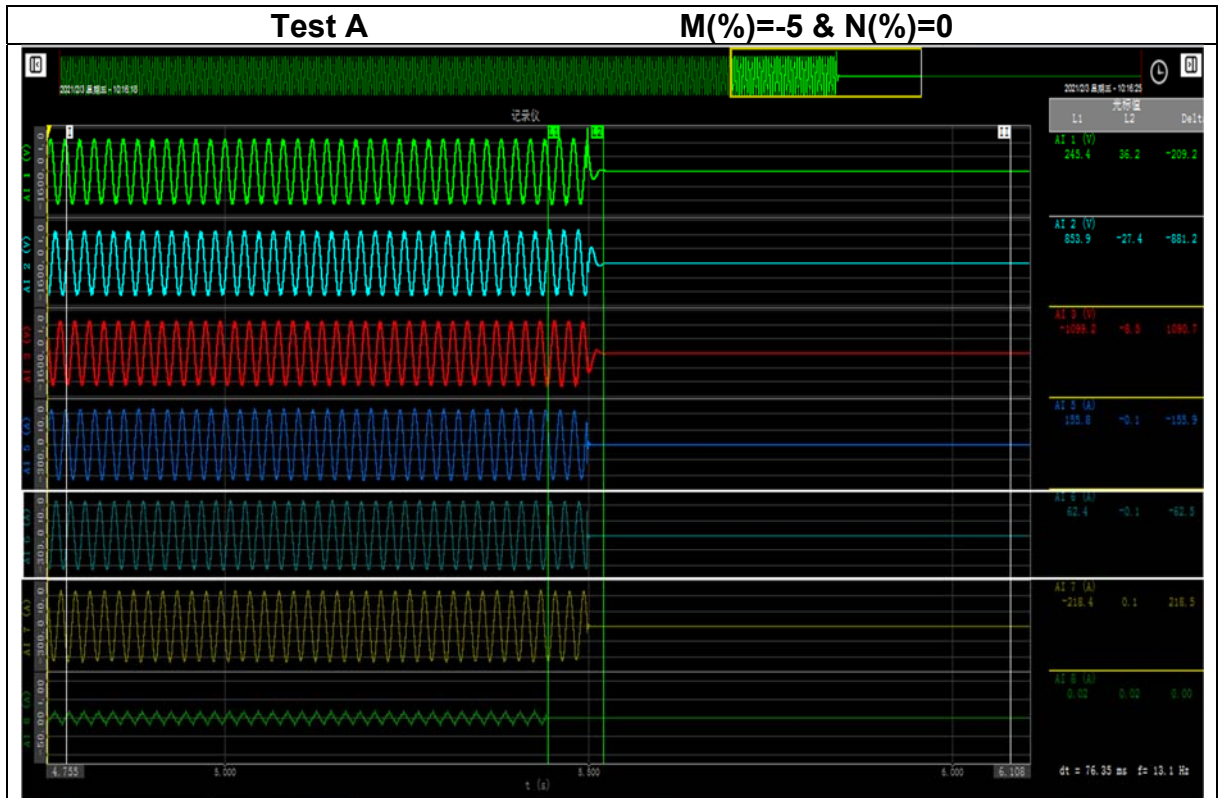


Test Condition C

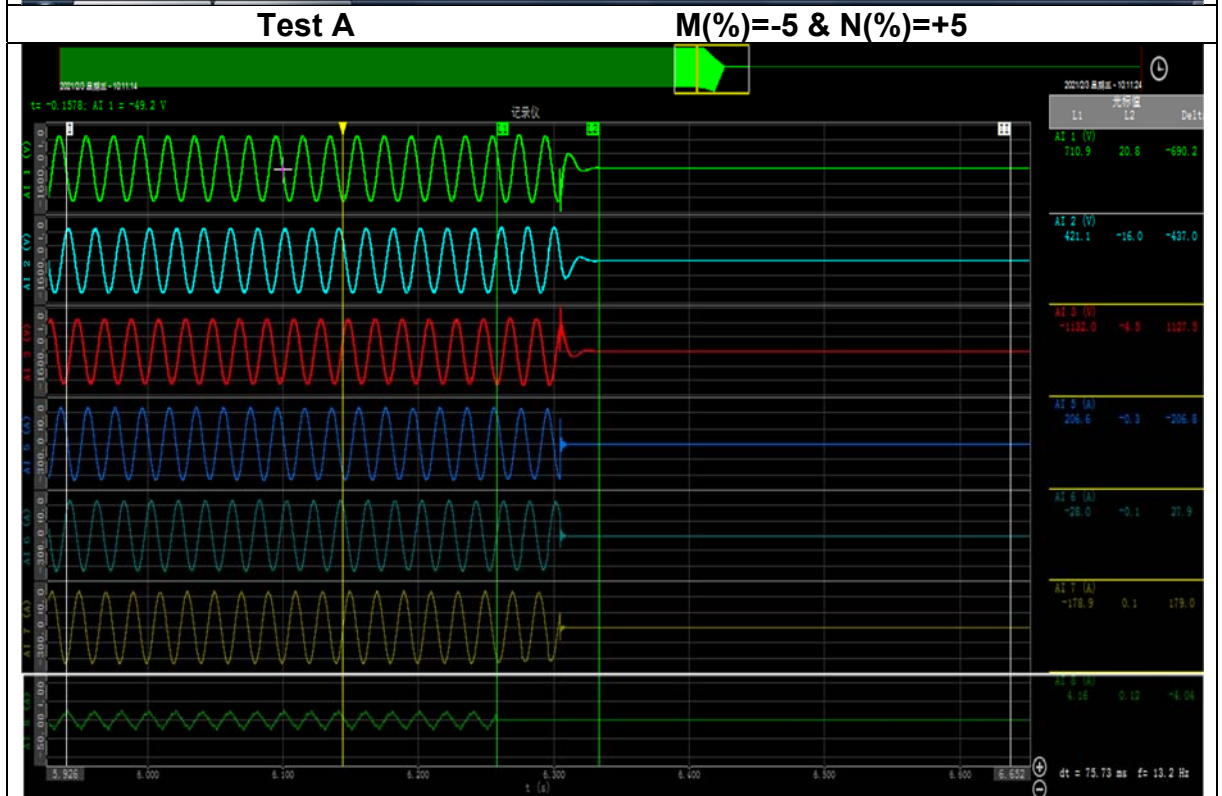
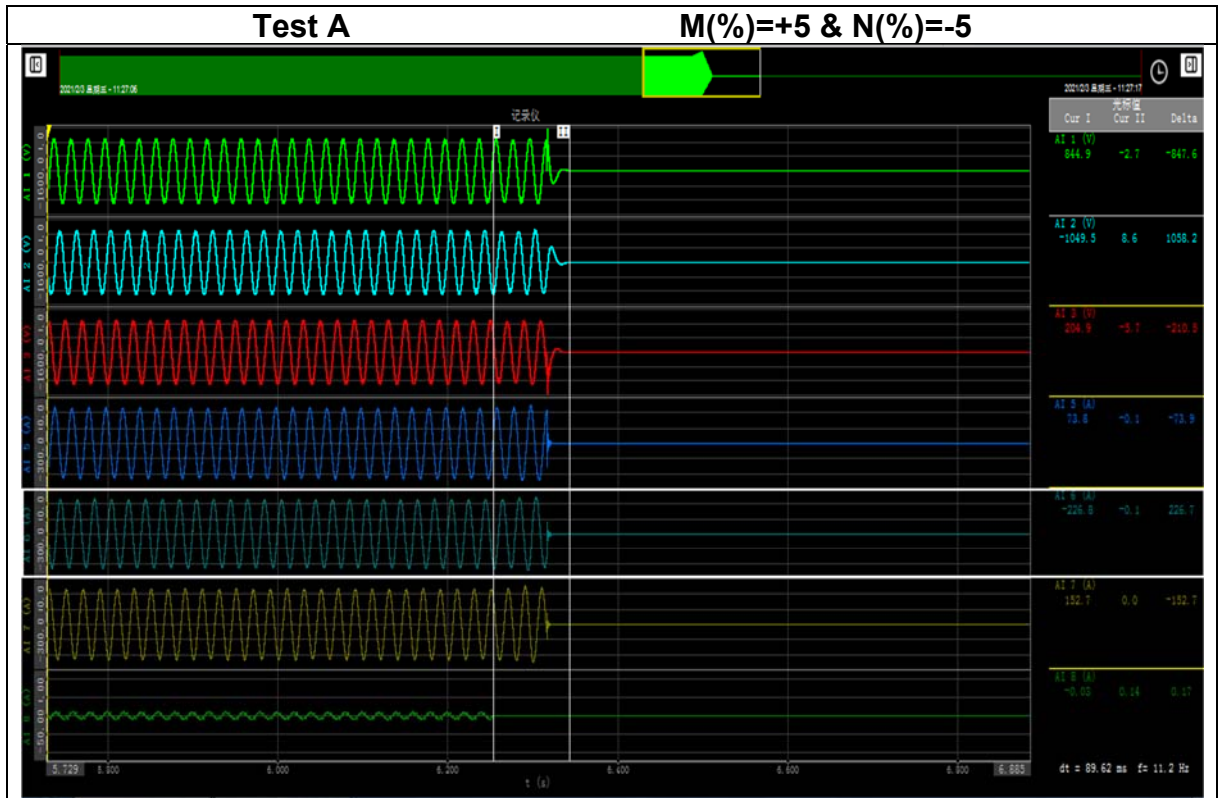


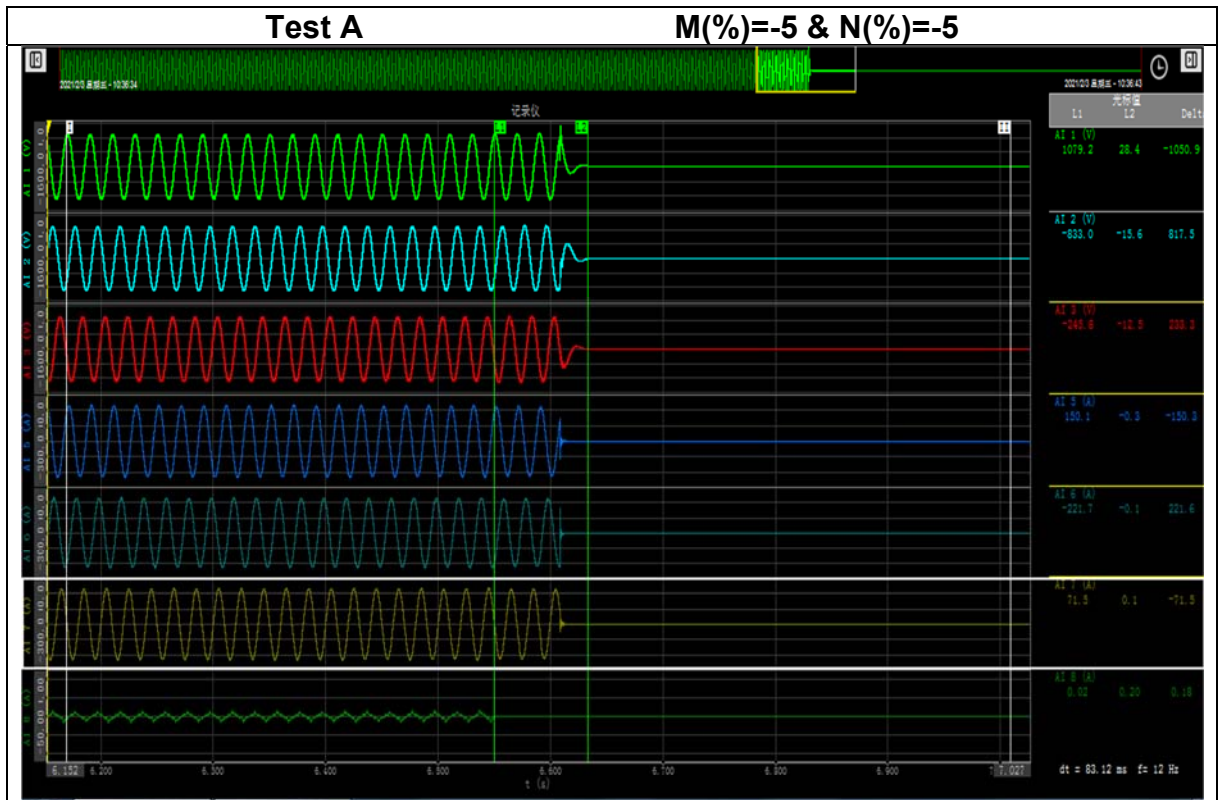


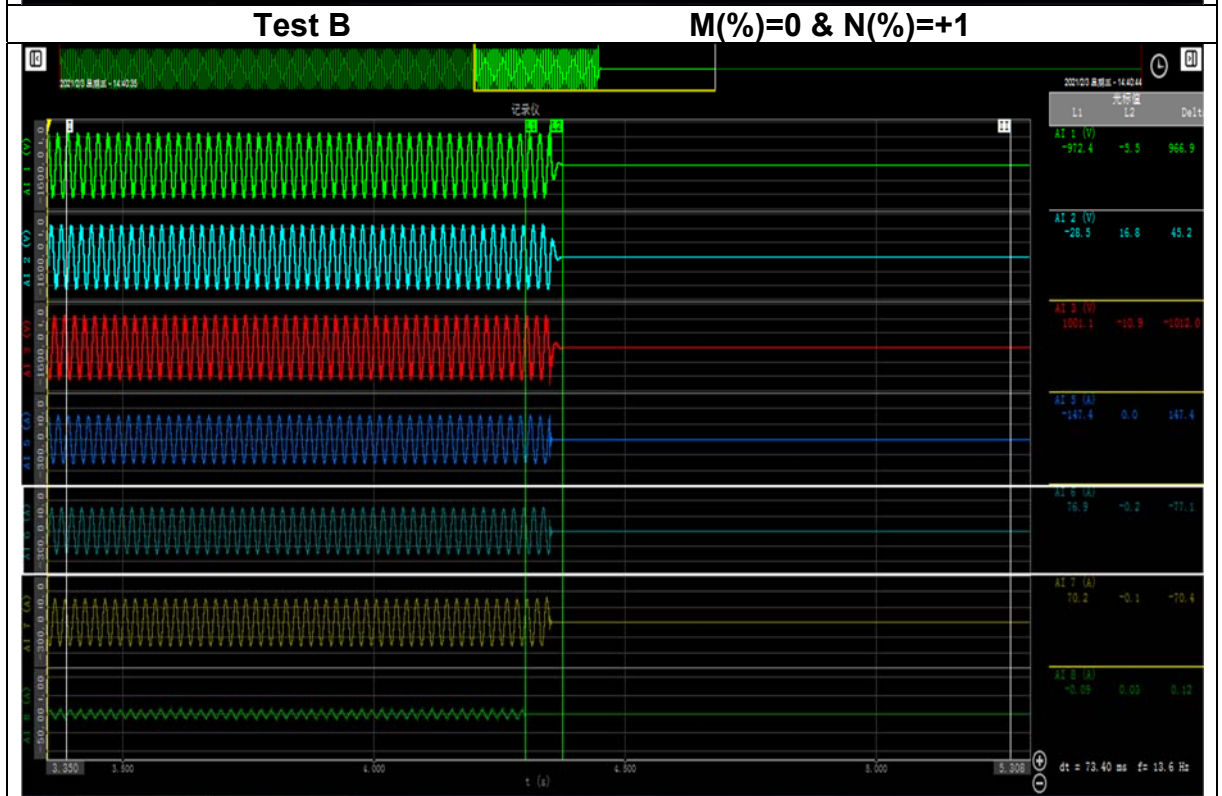
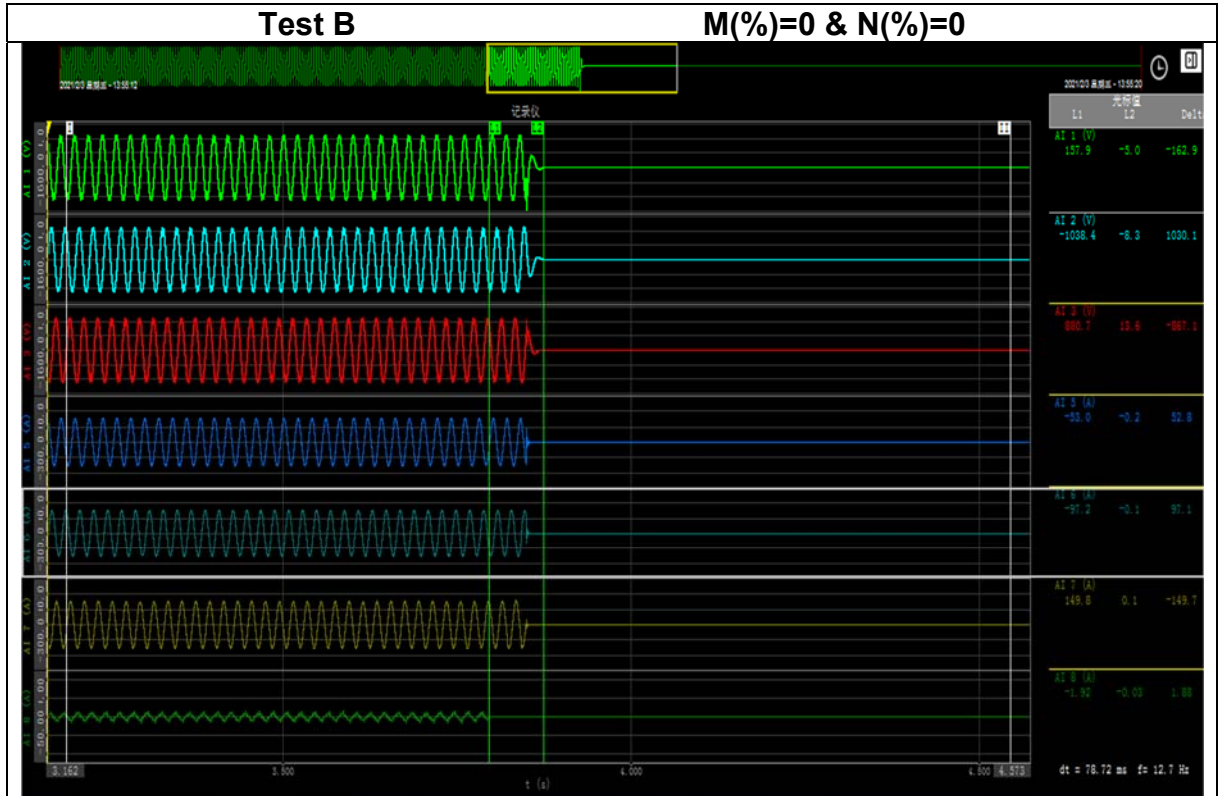


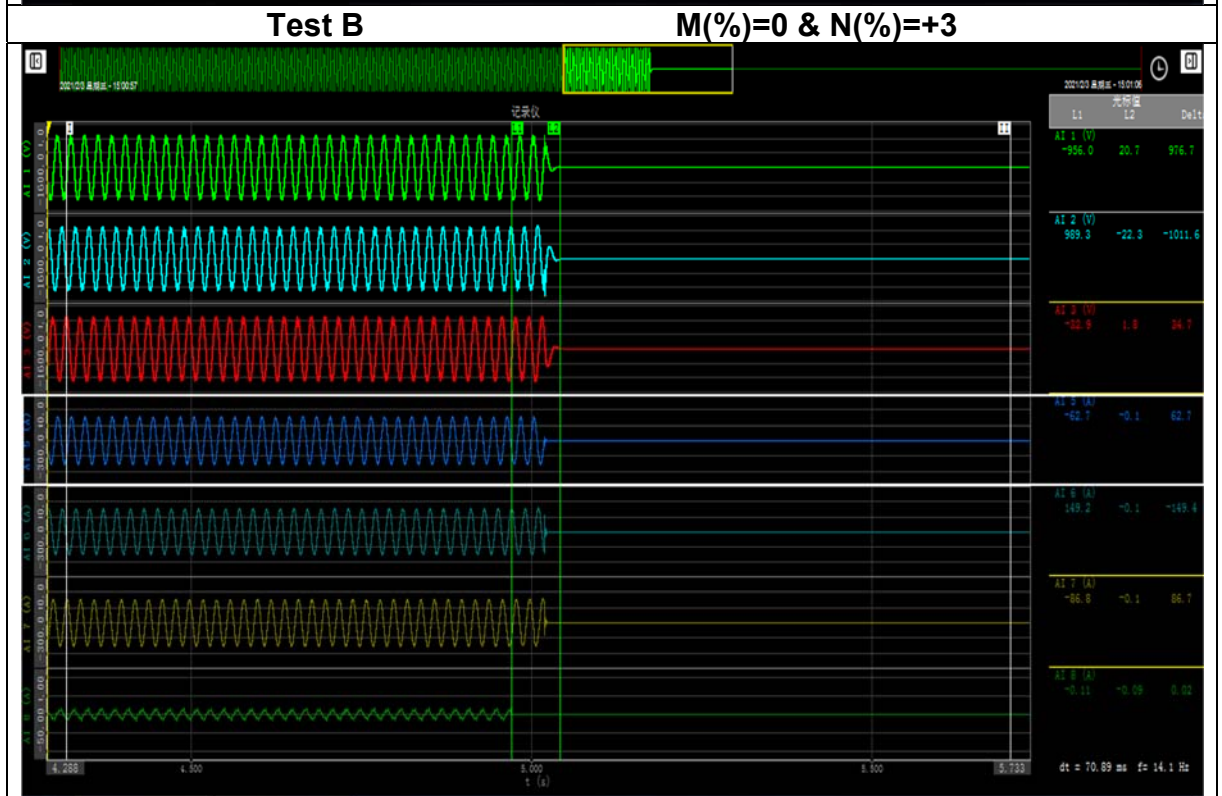
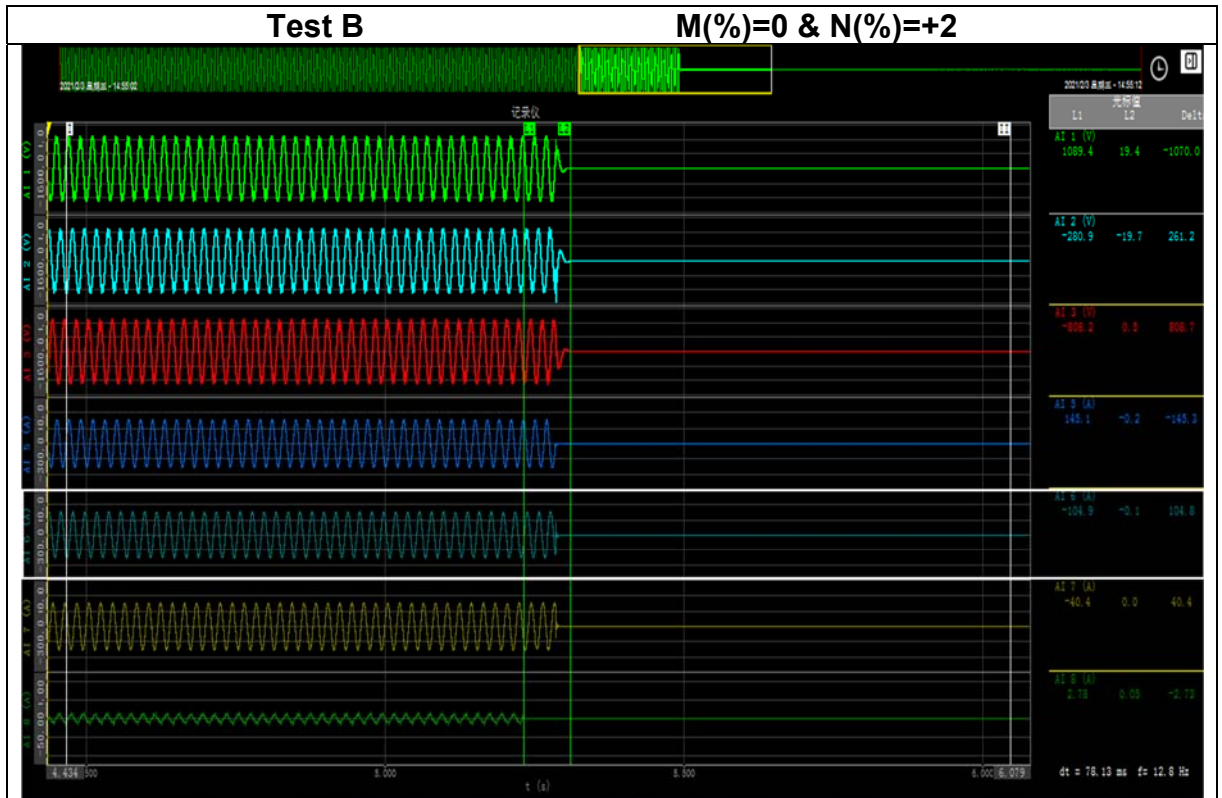


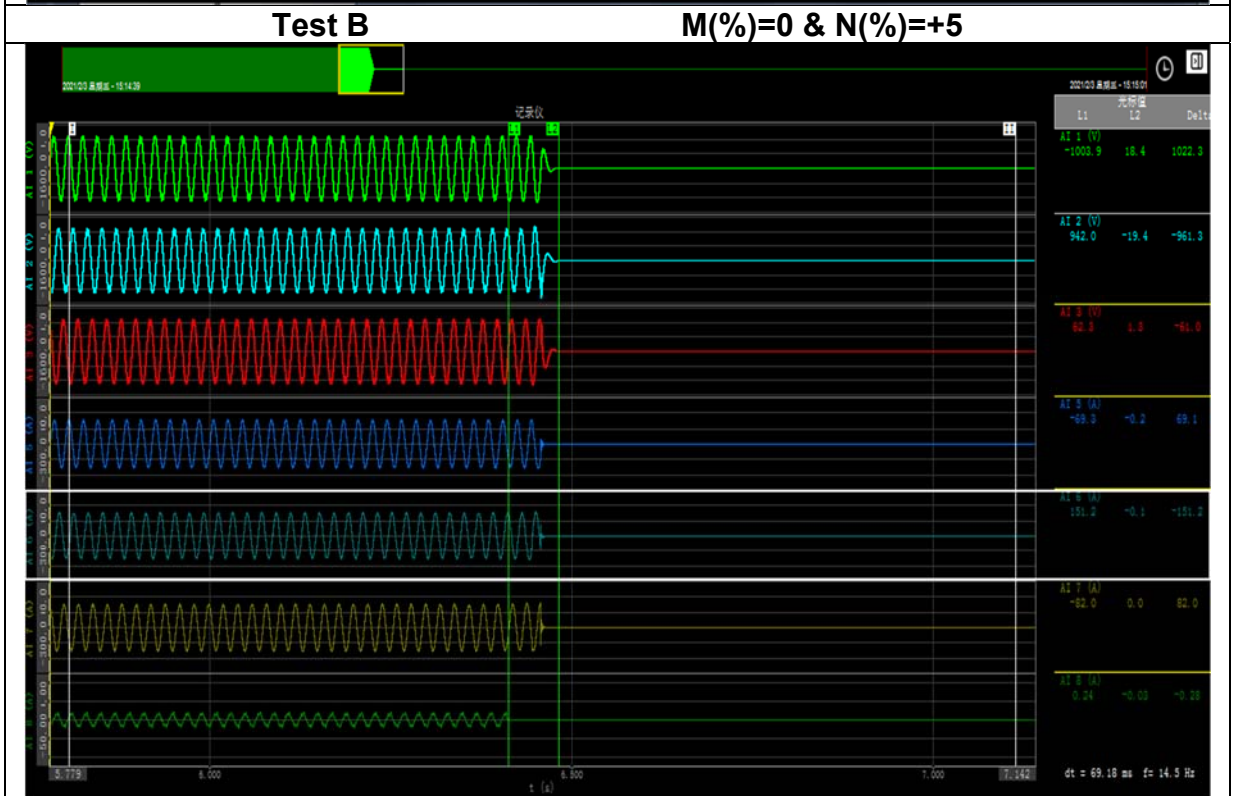
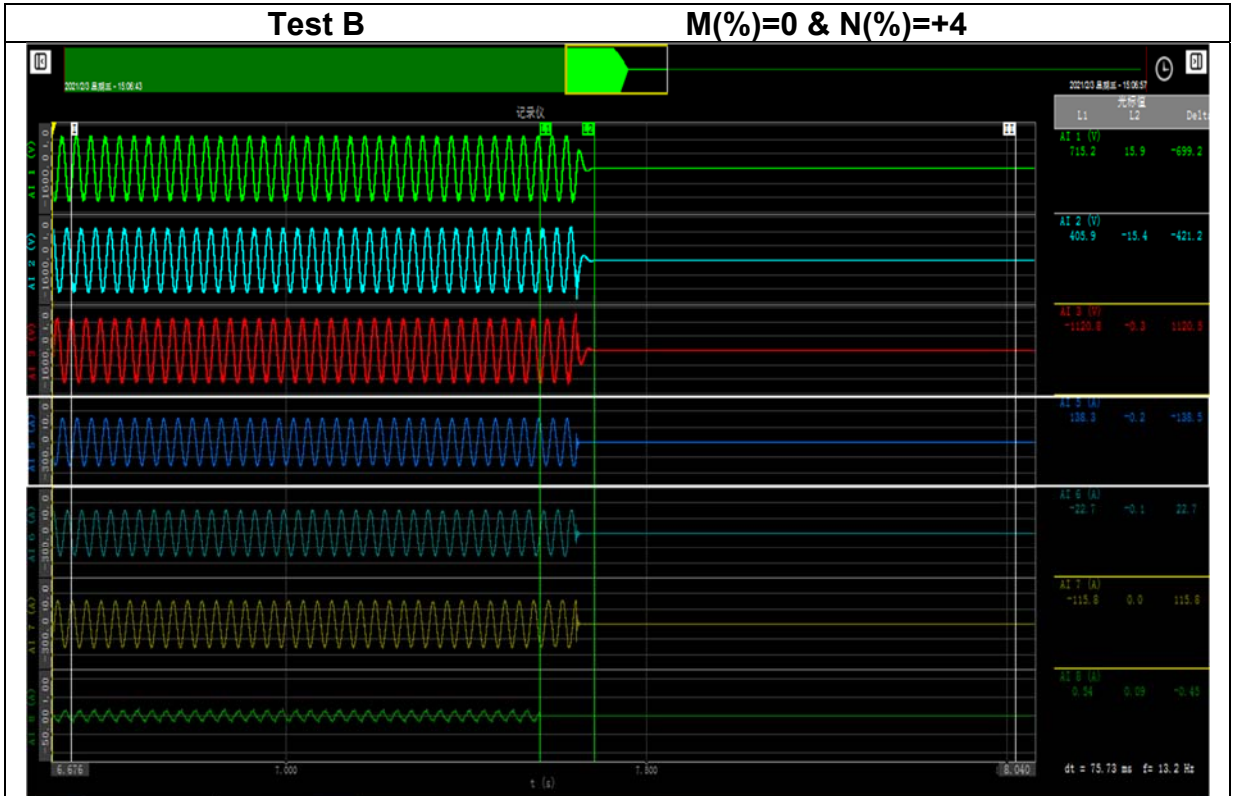


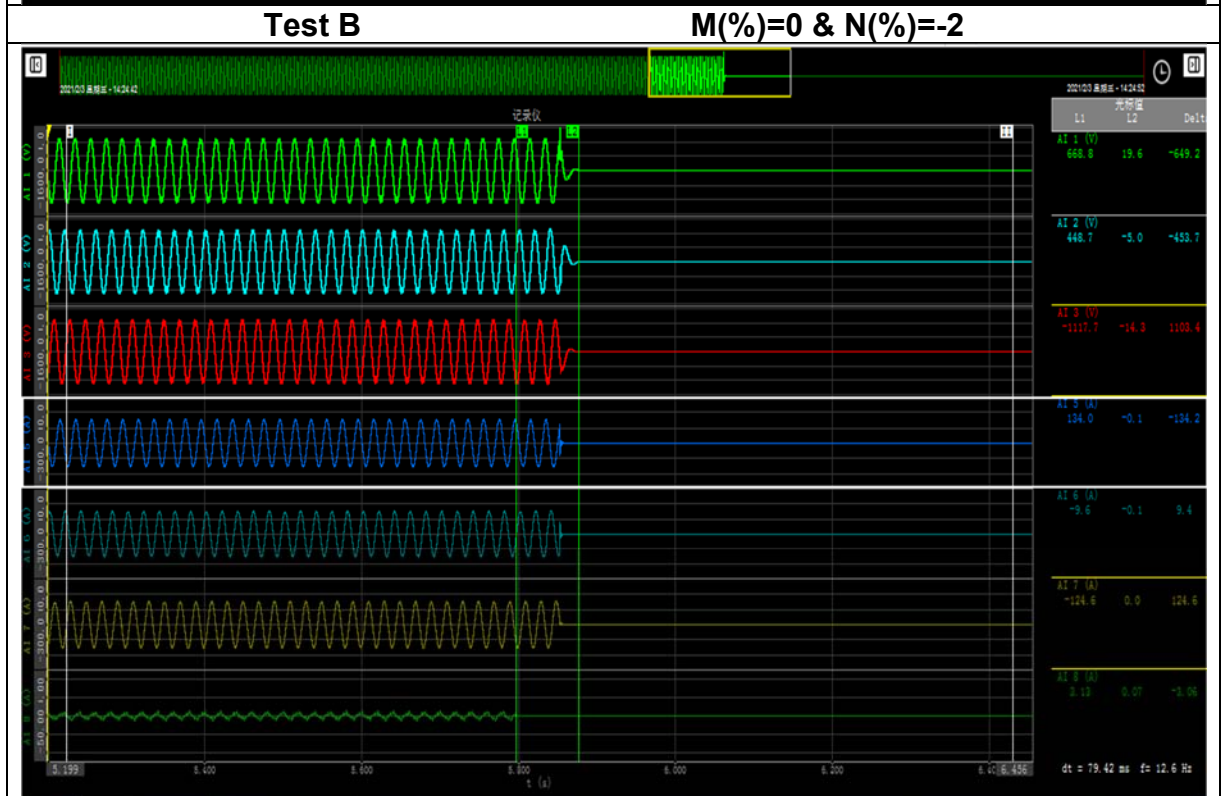
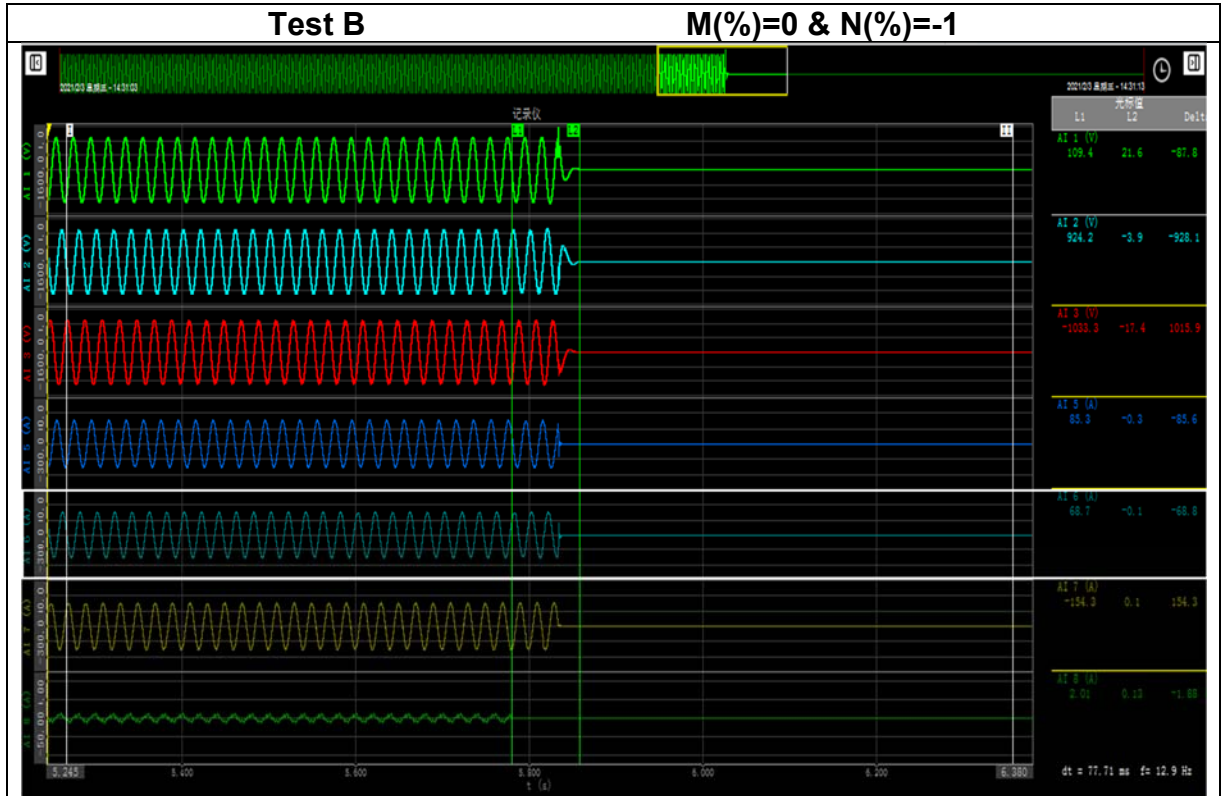


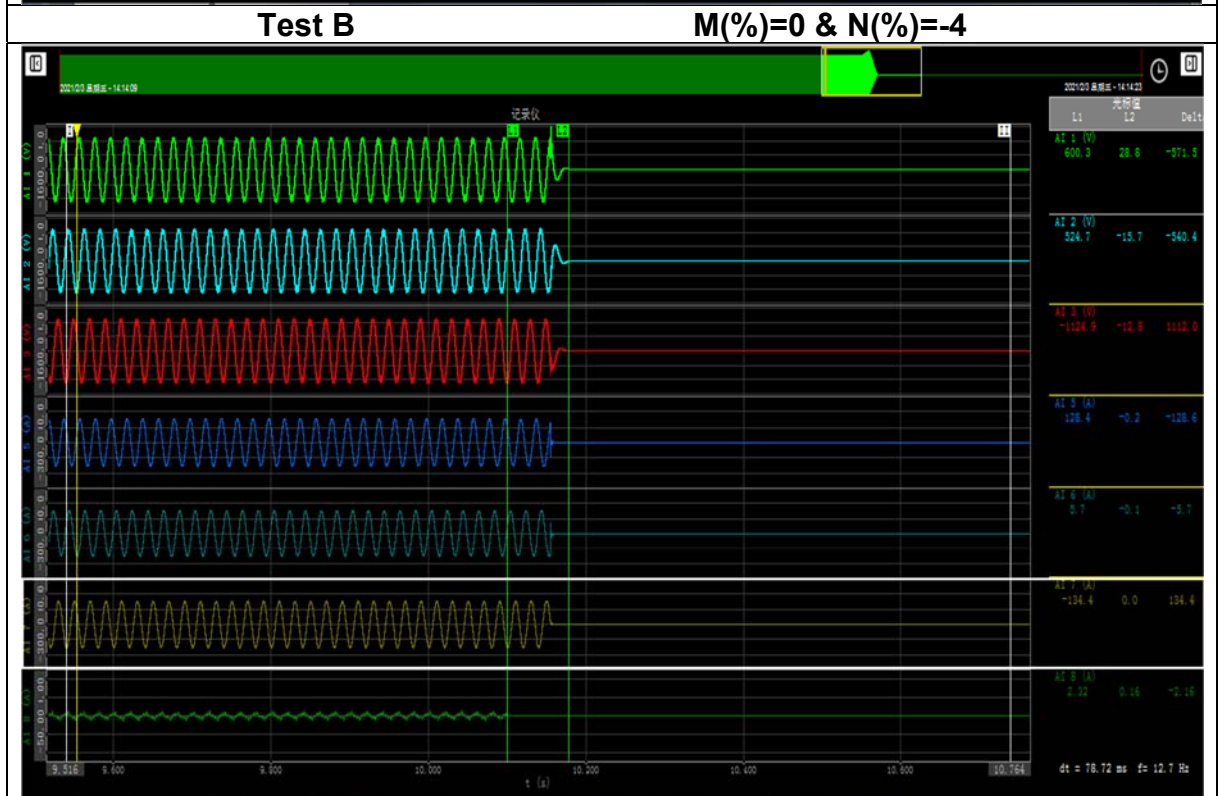
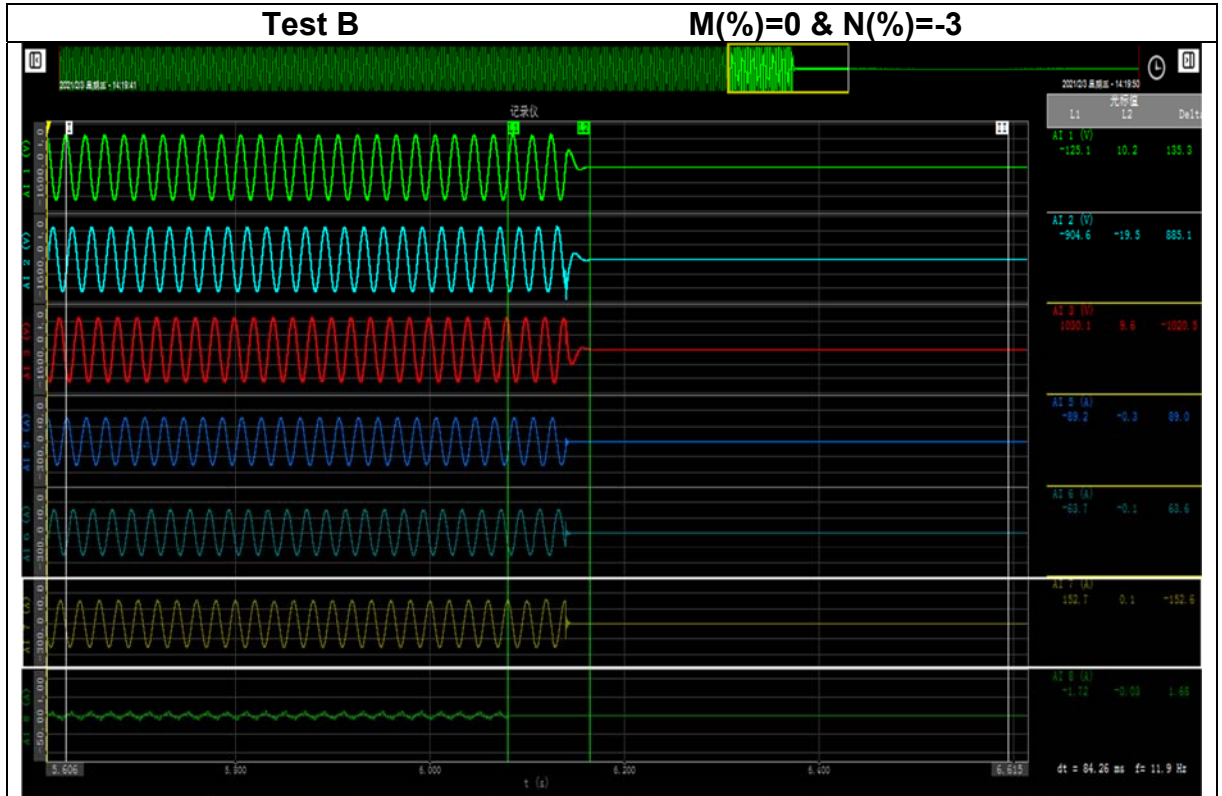


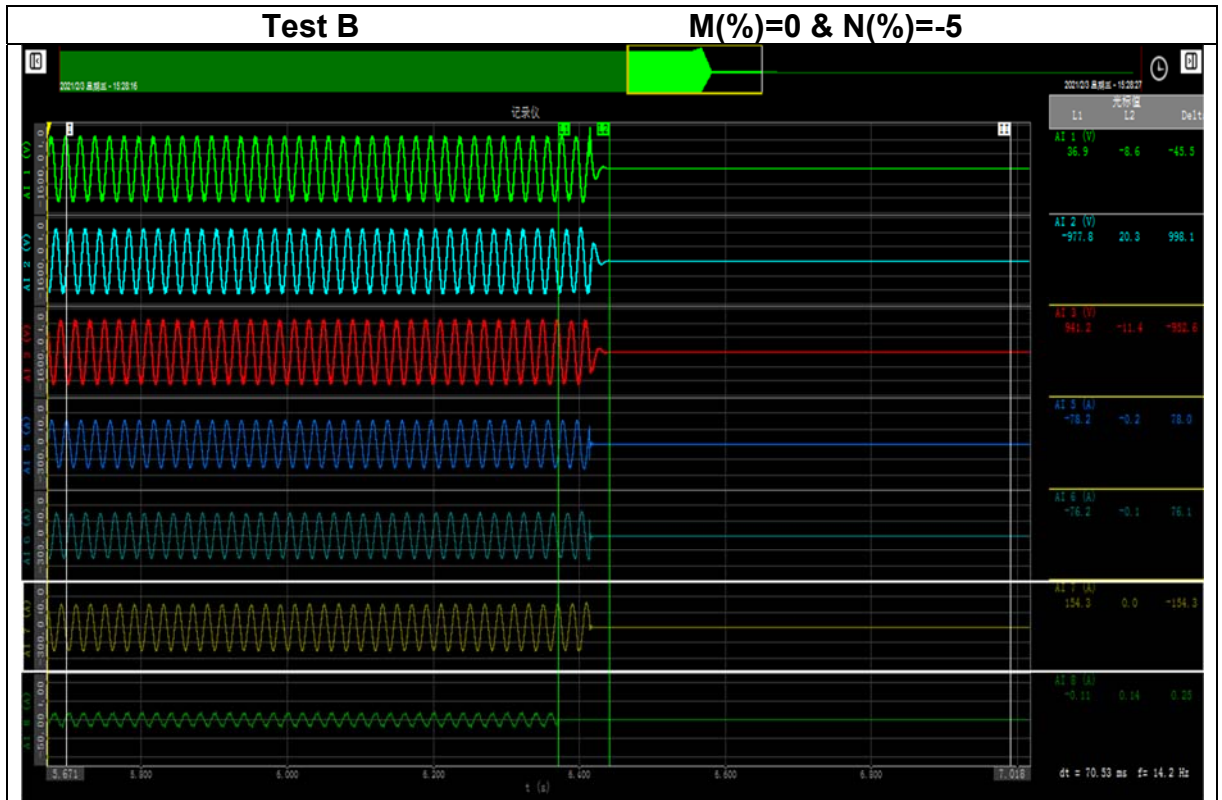




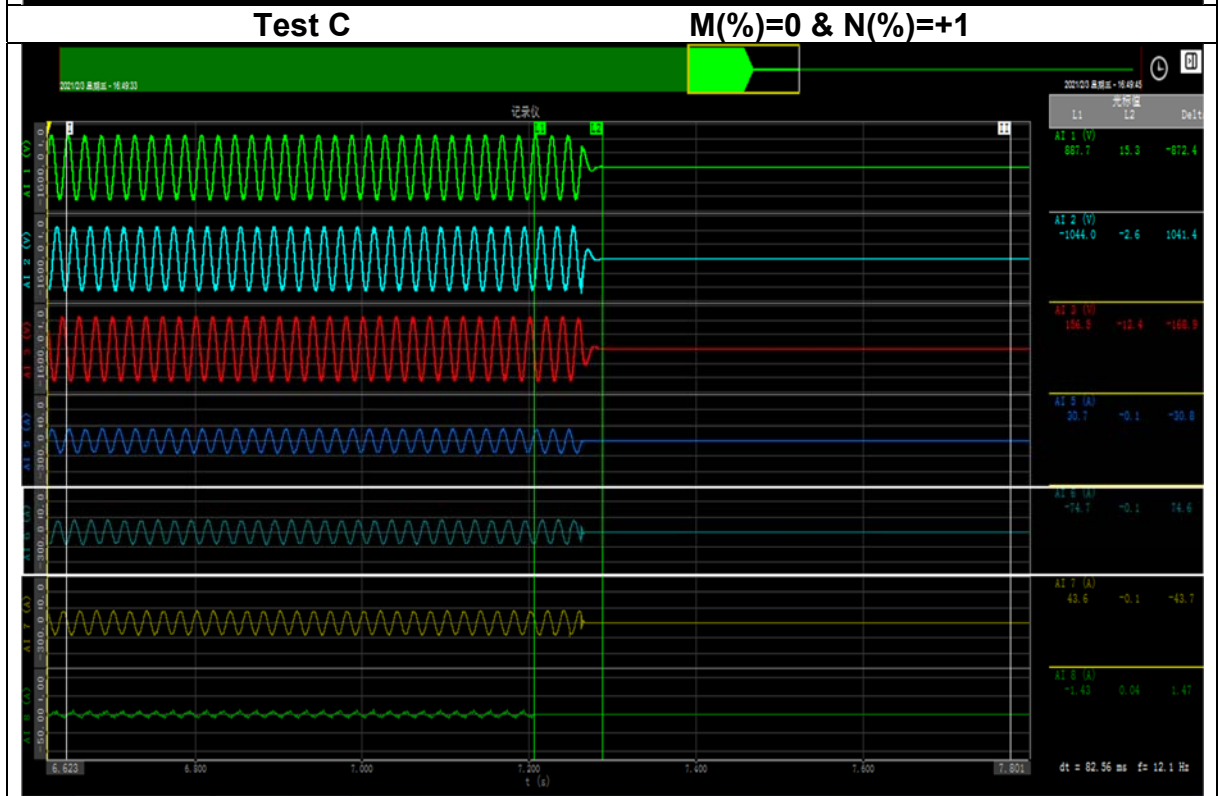
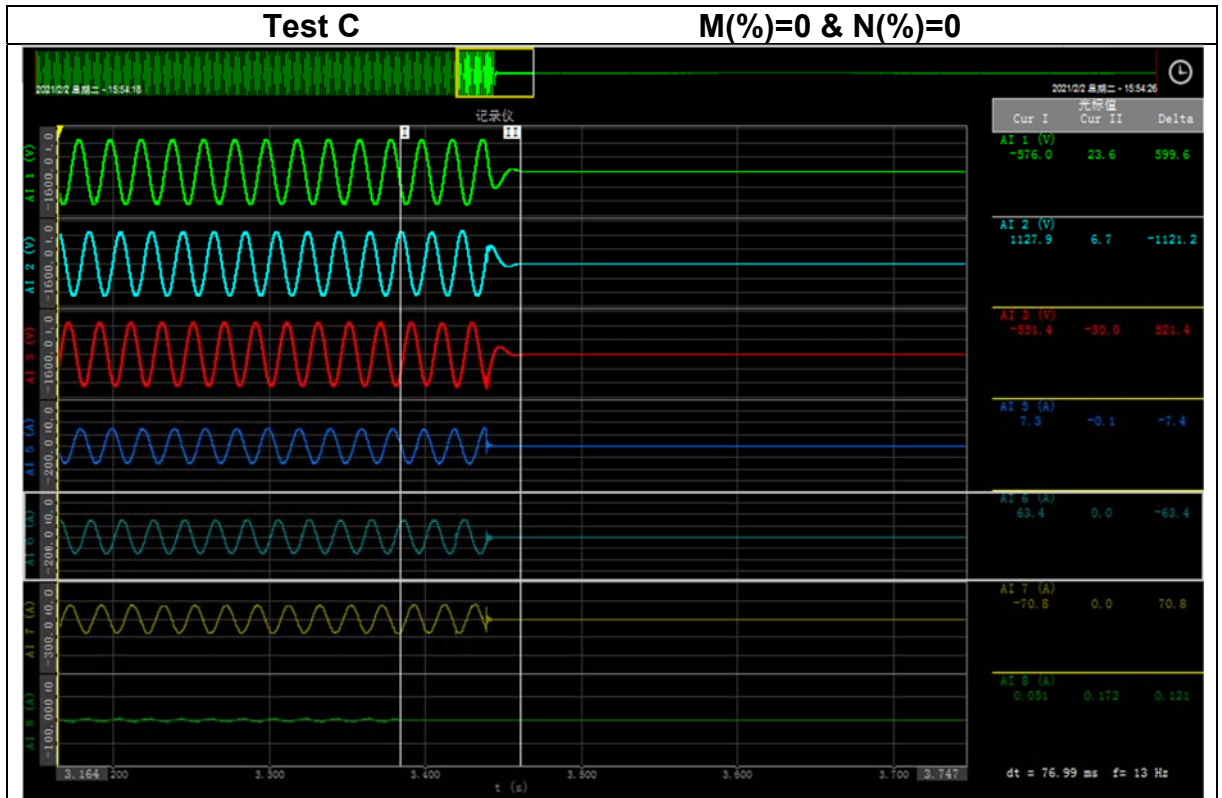


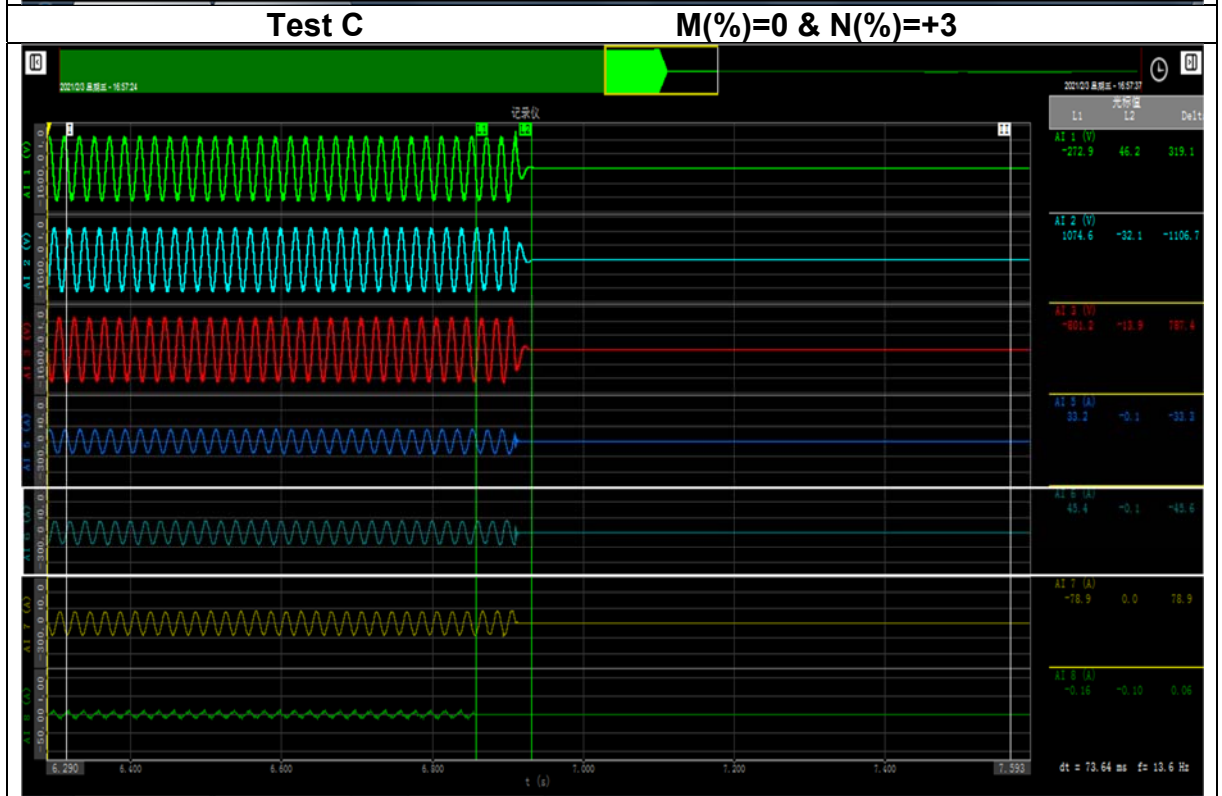
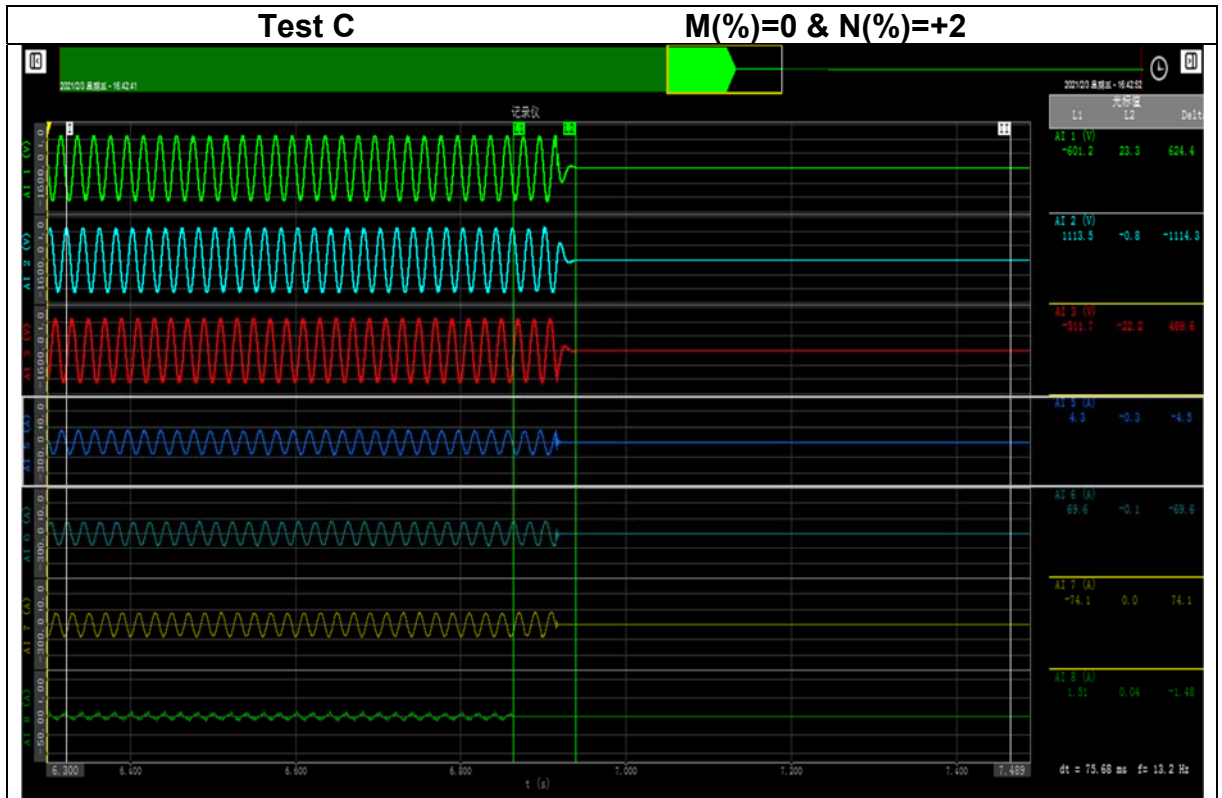


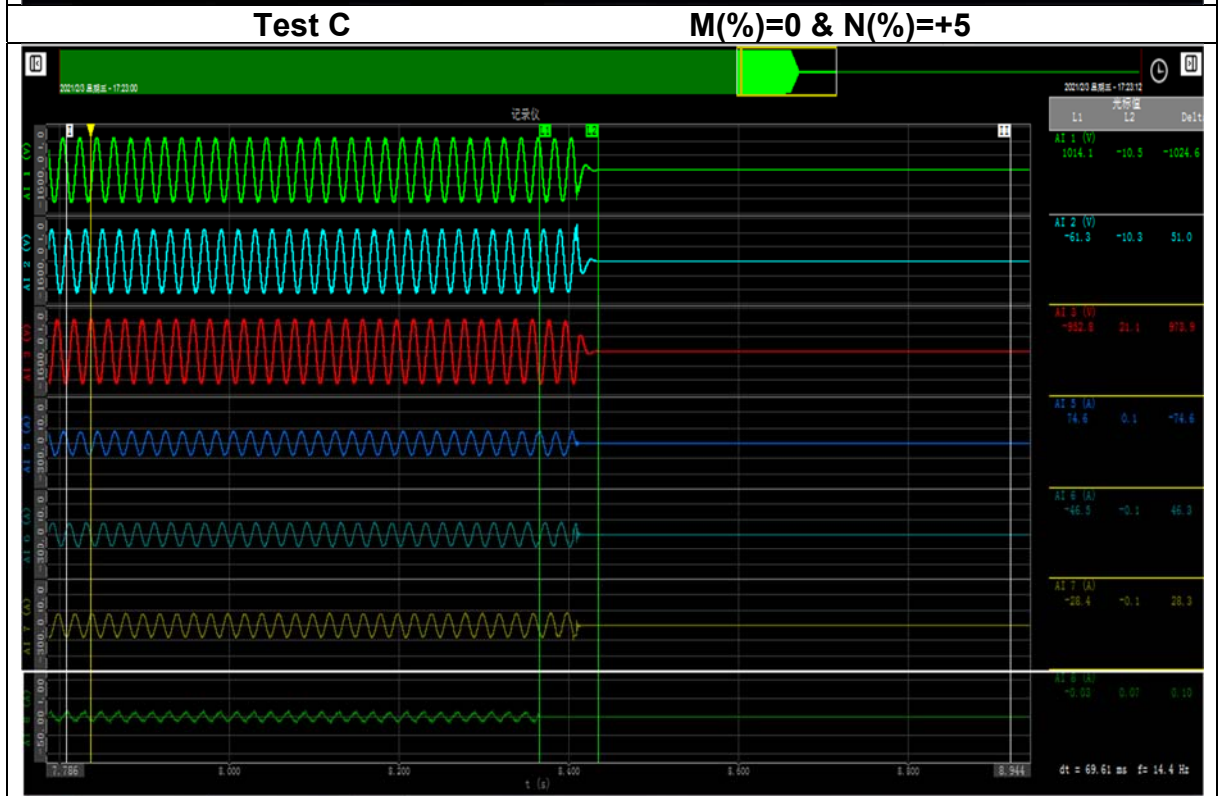
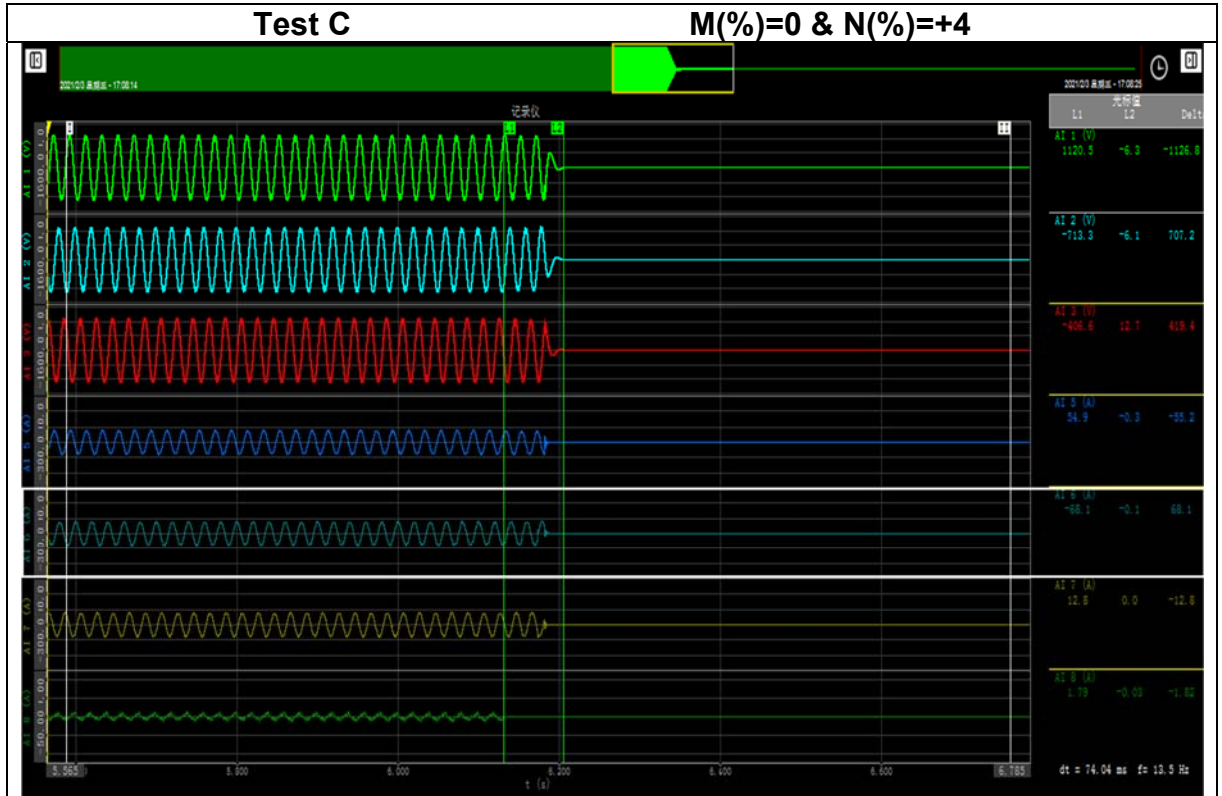


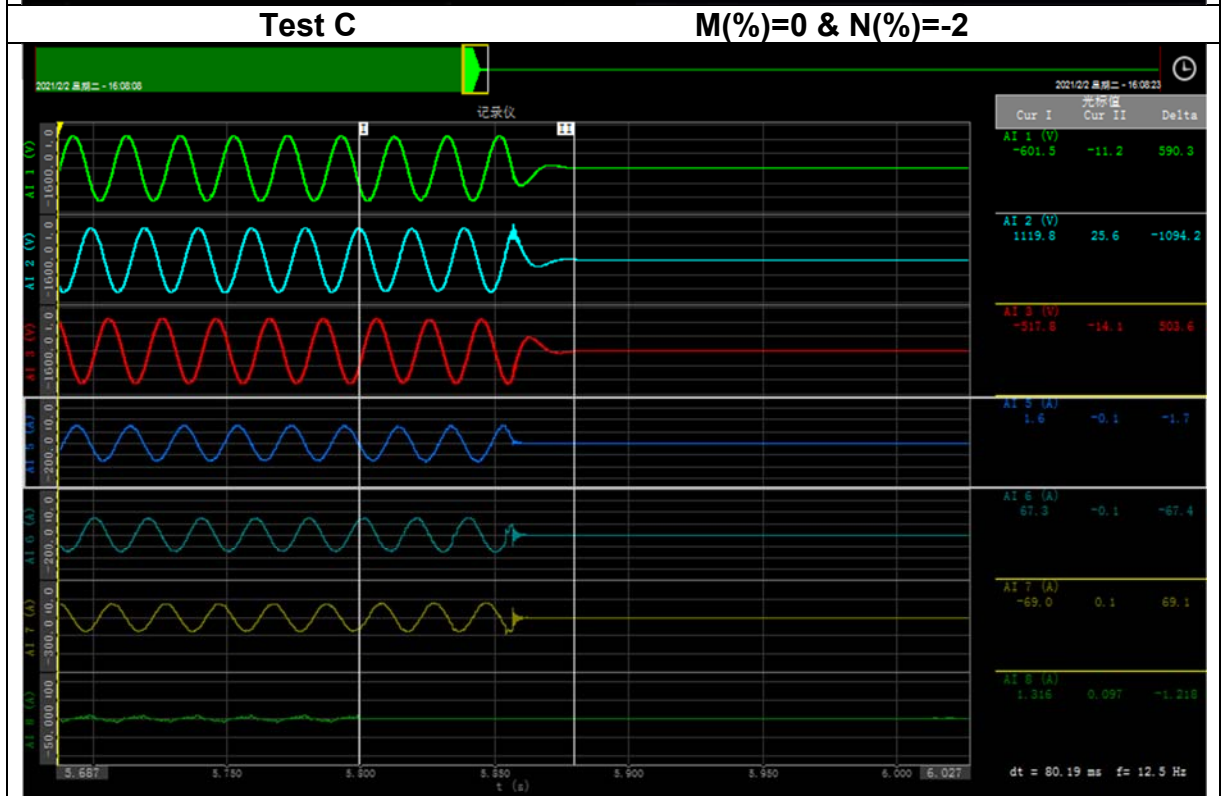
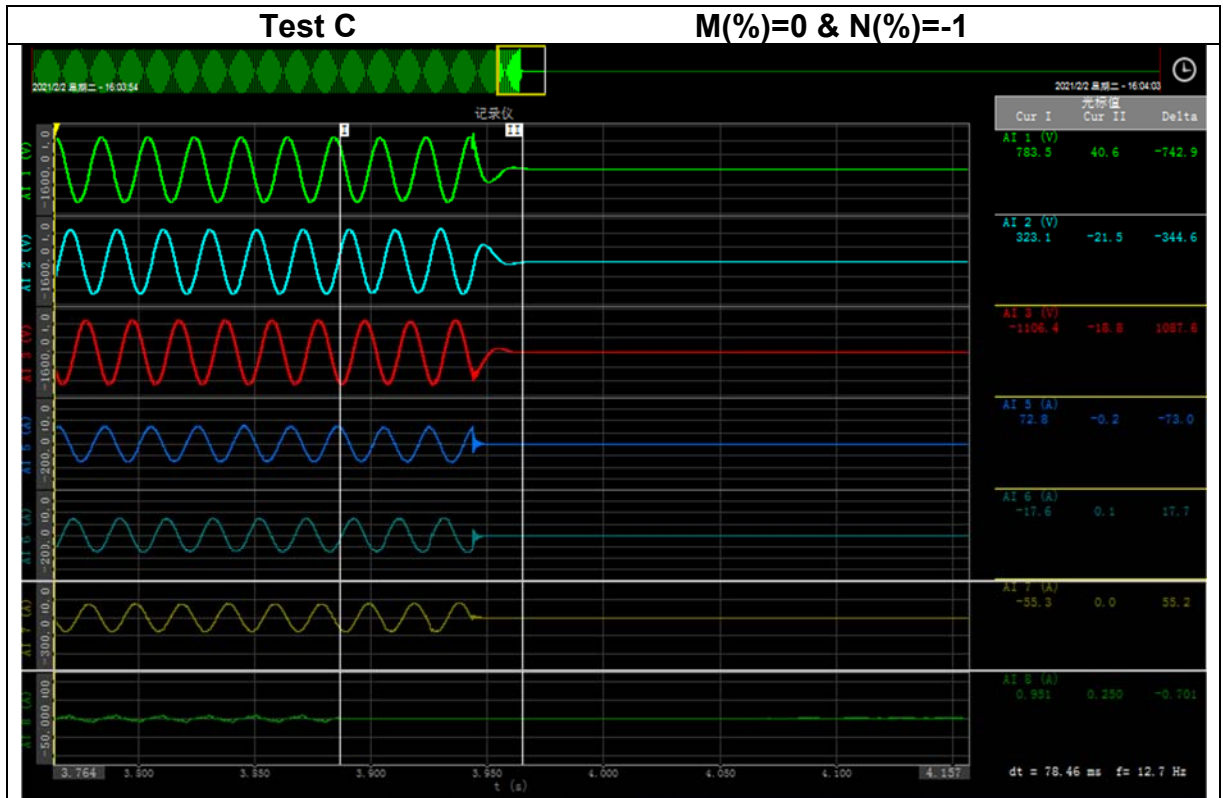


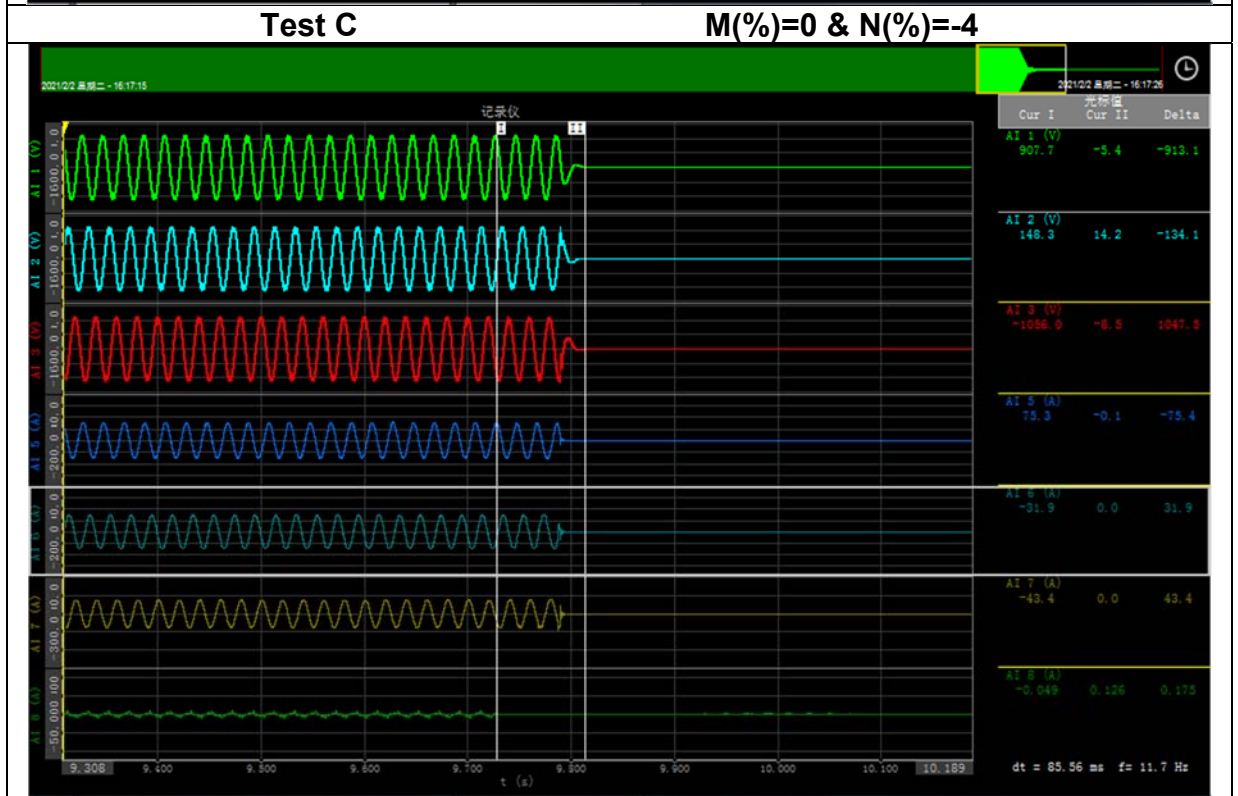
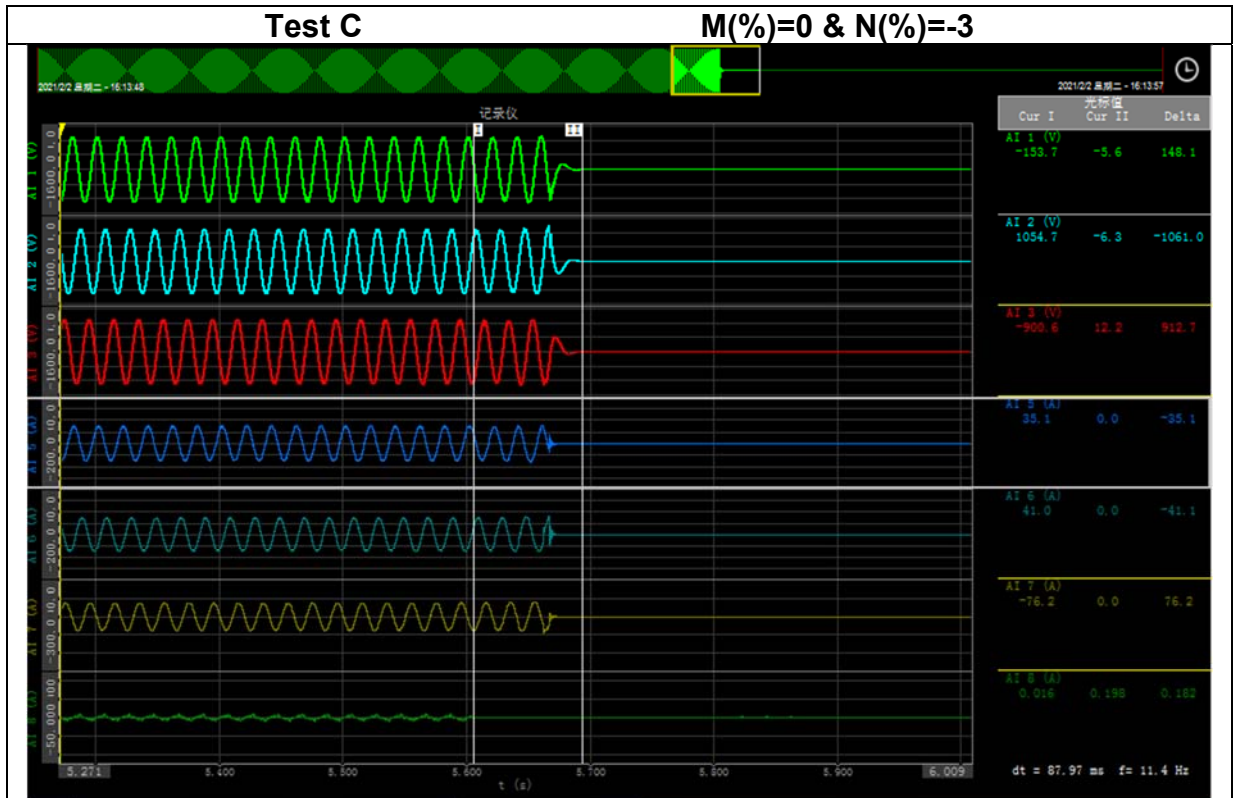


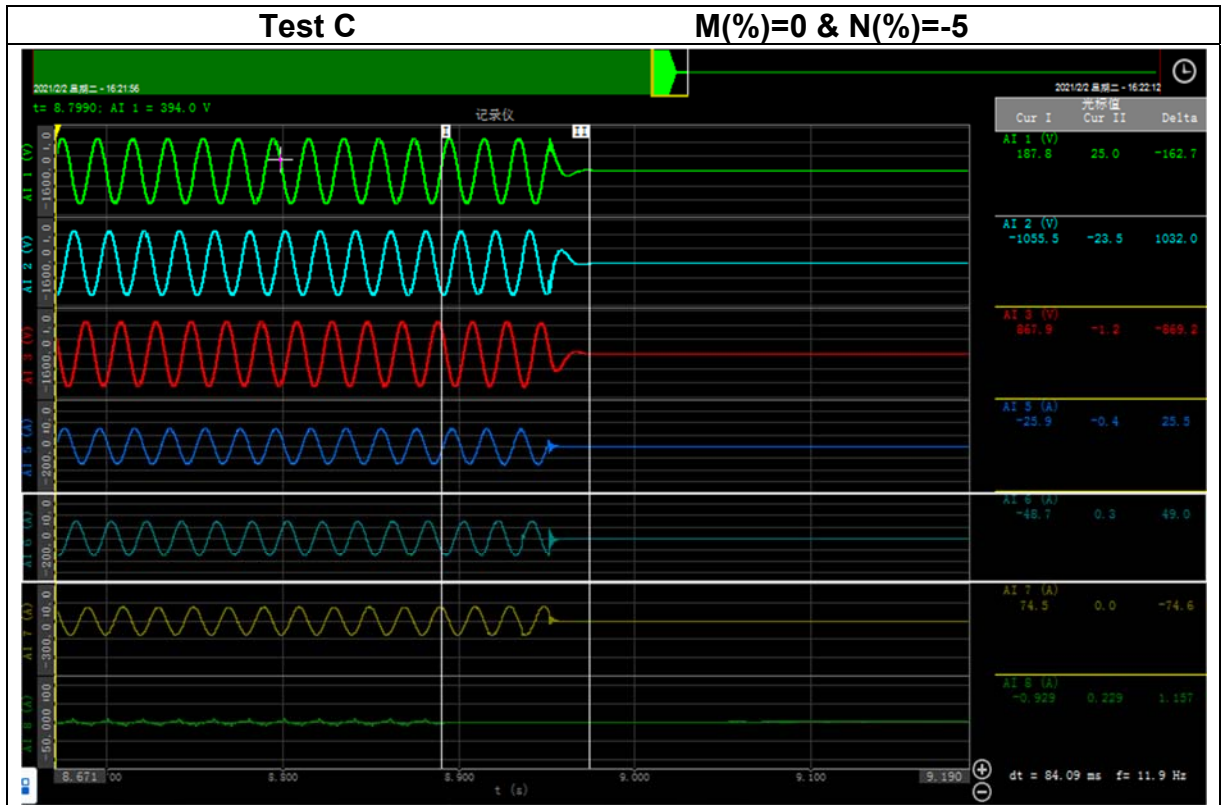












#### **4.3.4 Loss of Mains Protection, Vector Shift Stability test and RoCoF Stability test**

This test should be carried out in accordance with Annex A.7.1.2.6.

Four tests are required to be carried out with all protection functions enabled including loss of mains. For each stability test the Micro-generator should not trip during the test.

For the step change test the Power Generating Module should be operated with a measurable output at the start frequency and then a vector shift should be applied by extending or reducing the time of a single cycle with subsequent cycles returning to the start frequency. The start frequency should then be maintained for a period of at least 10 s to complete the test. The Power Generating Module should not trip during this test.

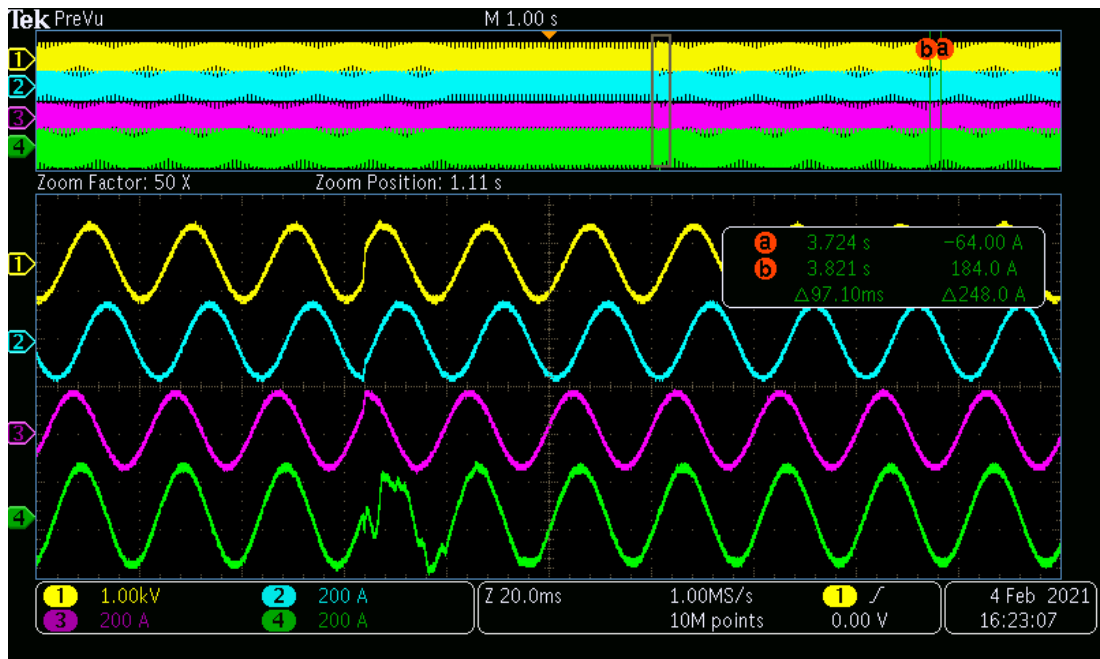
For frequency drift tests the Power Generating Module should be operated with a measurable output at the start frequency and then the frequency changed in a ramp function at 0.95 Hz/s to the end frequency. On reaching the end frequency it should be maintained for a period of at least 10s. The Power Generating Module should not trip during this test.

Test results are graphically shown in following pages.

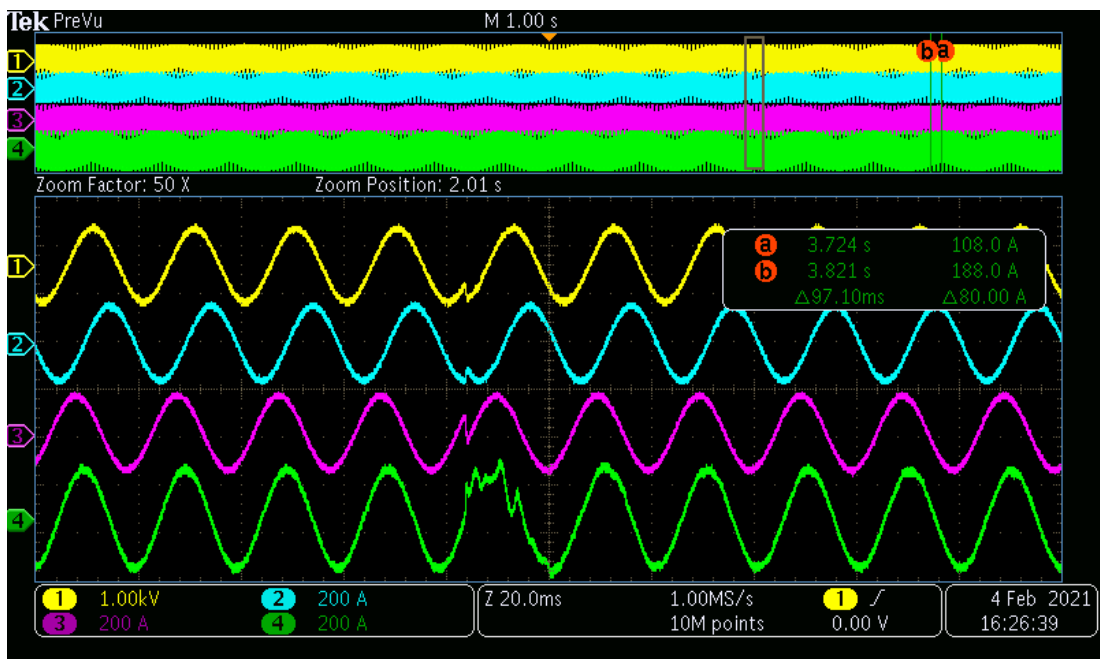
**Protection –Loss of Mains Protection, Vector Shift Stability test:** This test should be carried out in accordance with Annex A.7.1.2.6.

	Start Frequency	Change	Confirm no trip
Positive Vector Shift	49.5 Hz	+50 degrees	Pass
Negative Vector Shift	50.5 Hz	- 50 degrees	Pass

Positive Vector Shift:



Negative Vector Shift:



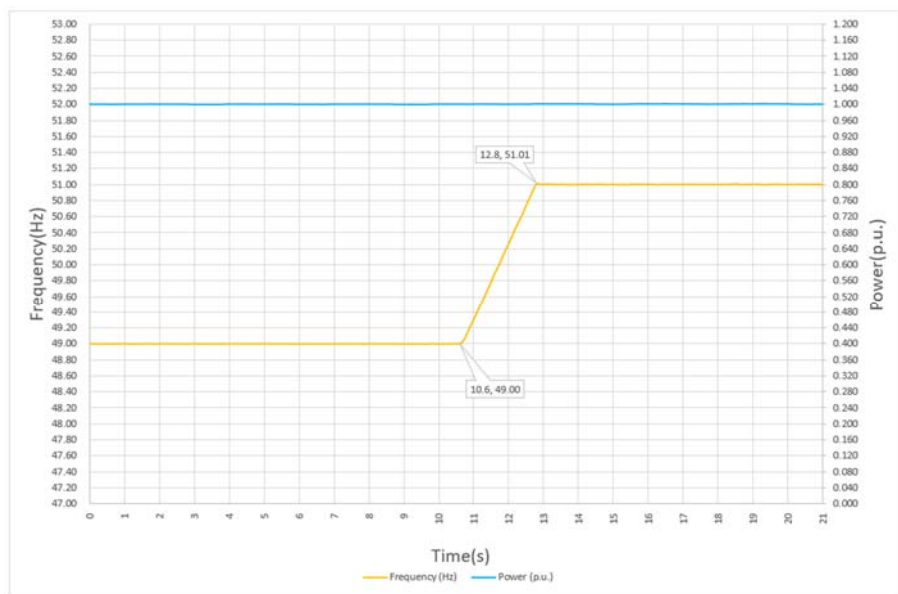


**Protection –Loss of Mains Protection, RoCoF Stability test:** This test should be carried out in accordance with Annex A.7.1.2.6.

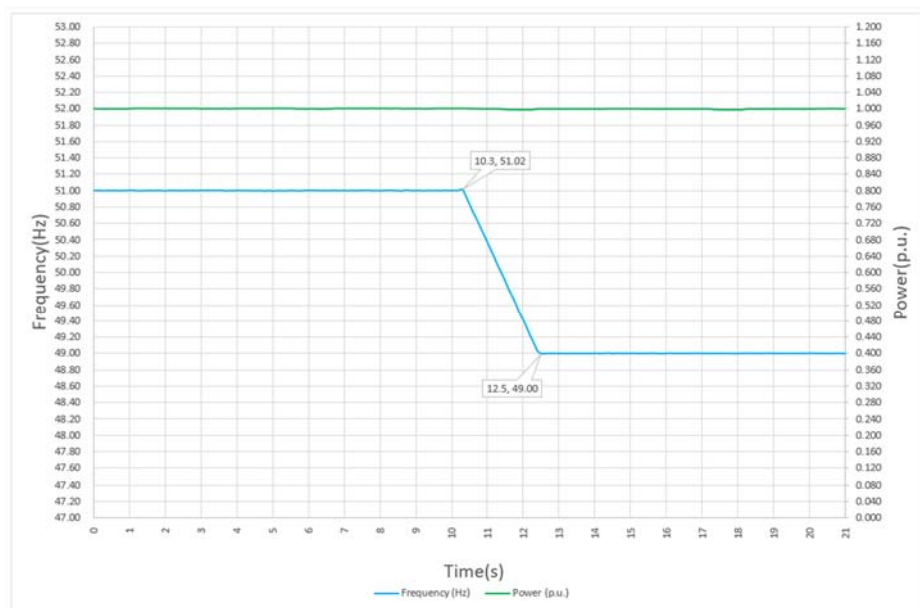
Ramp range	Test frequency ramp:	Test Duration	Confirm no trip
49.0 Hz to 51.0 Hz	+0.95 Hzs <sup>-1</sup>	2.2 s	Pass
51.0 Hz to 49.0 Hz	-0.95 Hzs <sup>-1</sup>	2.2 s	Pass

Test results are graphically shown in following pages.

+0.95 Hz/s:



-0.95 Hz/s:



**4.4 Limited Frequency Sensitive Mode - Overfrequency test**

This test should be carried out in accordance with Annex A.7.1.3.

The test should be carried out above 80% Registered Capacity and repeated at 40-60% Registered Capacity using the specific threshold frequency of 50.4 Hz and Droop of 10%.

The Power Park Module should be tested at the following frequencies:

- Step a) 50.00 Hz  $\pm$ 0.01 Hz
- Step b) 50.45 Hz  $\pm$ 0.05 Hz
- Step c) 50.70 Hz  $\pm$ 0.10 Hz
- Step d) 51.15 Hz  $\pm$ 0.05 Hz
- Step e) 50.70 Hz  $\pm$ 0.10 Hz
- Step f) 50.45 Hz  $\pm$ 0.05 Hz
- Step g) 50.00 Hz  $\pm$ 0.01 Hz

The frequency at each step should be maintained for at least one minute and the Active Power reduction in the form of a gradient determined and assessed for compliance with paragraph 11.2.3.

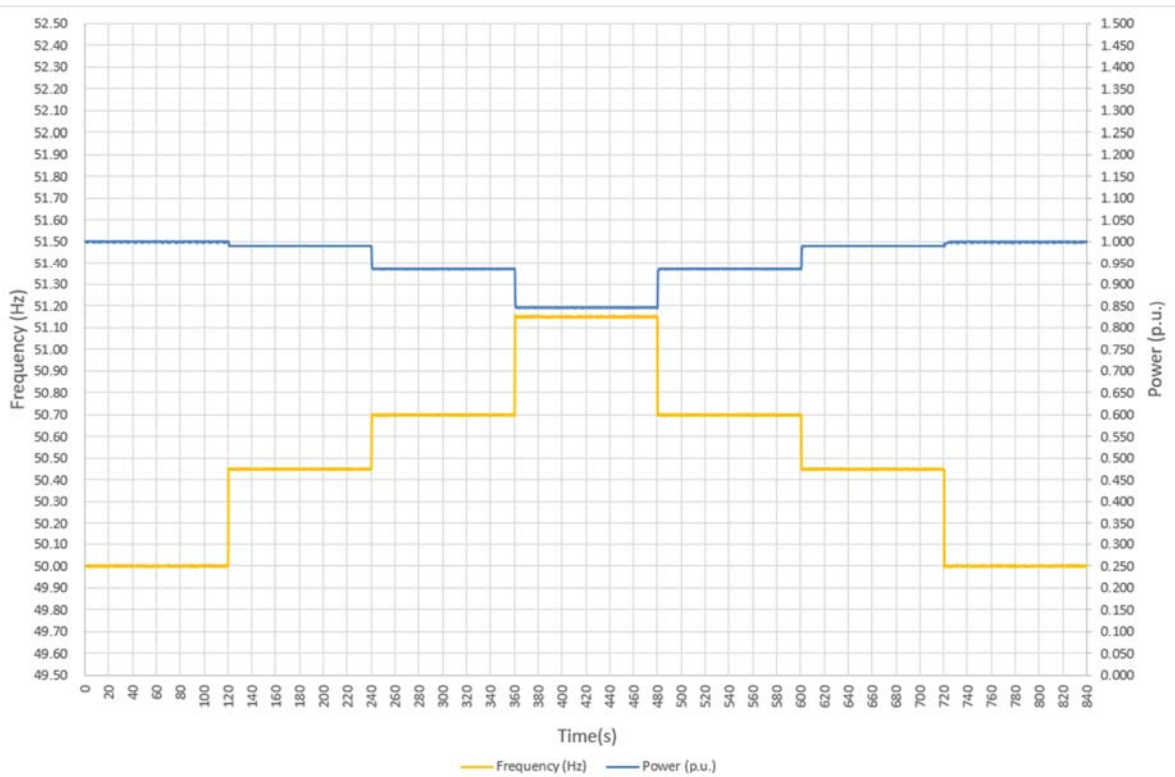
Following tables show the test results:

Test sequence at Registered Capacity >80%	Measured Active Power Output (W)	Frequency (Hz)	Primary Power Source	Active Power Gradient (%)
Step a) 50.00 Hz $\pm$ 0.01 Hz	135968	50.00	DC Souce	N/A
Step b) 50.45 Hz $\pm$ 0.05 Hz	134694	50.45		10.7
Step c) 50.70 Hz $\pm$ 0.10 Hz	127170	50.70		9.3
Step d) 51.15 Hz $\pm$ 0.05 Hz	115009	51.15		9.7
Step e) 50.70 Hz $\pm$ 0.10 Hz	127187	50.70		9.3
Step f) 50.45 Hz $\pm$ 0.05 Hz	134688	50.45		10.6
Step g) 50.00 Hz $\pm$ 0.01 Hz	135906	50.00		N/A

Test sequence at Registered Capacity 40% - 60%	Measured Active Power Output (W)	Frequency (Hz)	Primary Power Source	Active Power Gradient (%)
Step a) 50.00 Hz $\pm$ 0.01 Hz	68068	50.00	DC Souce	N/A
Step b) 50.45 Hz $\pm$ 0.05 Hz	67431	50.45		10.7
Step c) 50.70 Hz $\pm$ 0.10 Hz	63584	50.70		9.1
Step d) 51.15 Hz $\pm$ 0.05 Hz	57495	51.15		9.7
Step e) 50.70 Hz $\pm$ 0.10 Hz	63583	50.70		9.1
Step f) 50.45 Hz $\pm$ 0.05 Hz	67387	50.45		10.0
Step g) 50.00 Hz $\pm$ 0.01 Hz	68076	50.00		N/A

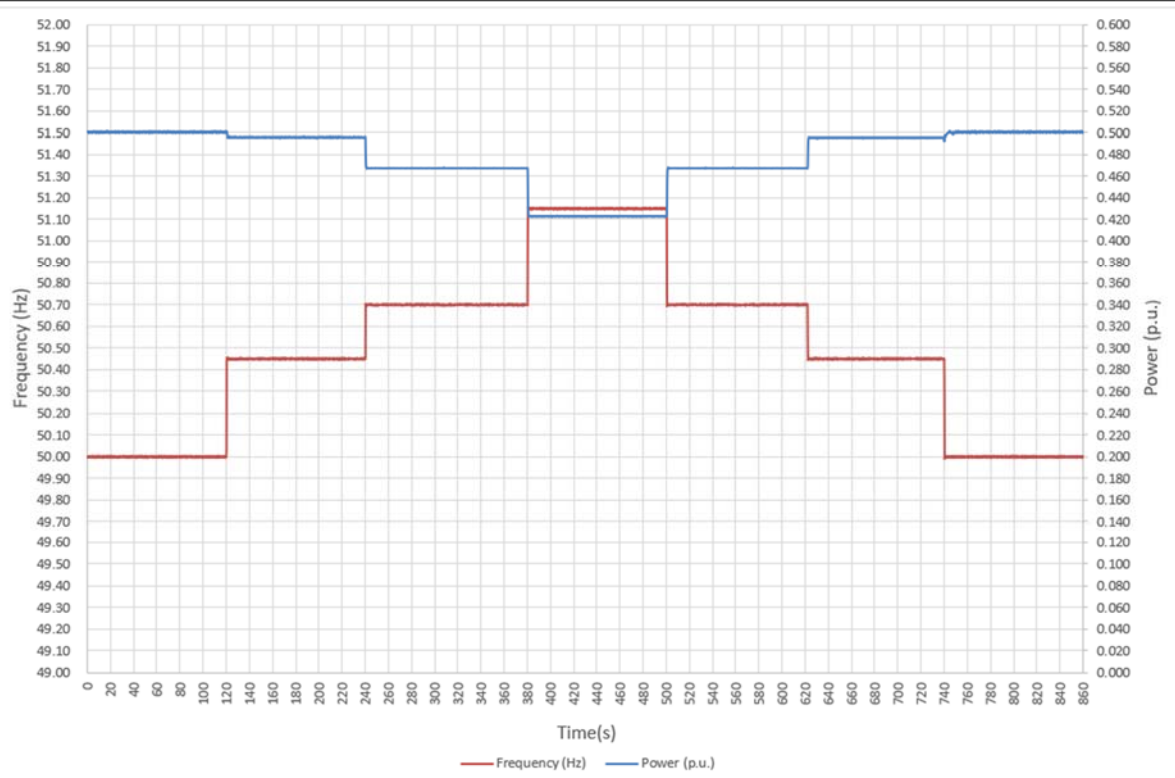
Test results are graphically shown in following pages.

**Over-frequency curve (droop of 10 % at 100% Pn)**



Remark: Test for frequency threshold 50.4Hz with droop 10%, intentional delay is setting to 0s.

**Over-frequency curve (droop of 10 % at 50% Pn)**



Remark: Test for frequency threshold 50.4Hz with droop 10%, intentional delay is setting to 0s.

#### 4.5 Re-connection timer

Test should prove that the reconnection sequence starts after a minimum delay of 20 s for restoration of voltage and frequency to within the stage 1 settings of Table 10.1.

The evaluation of this point has been made according to Annex A.7.2.2.5.

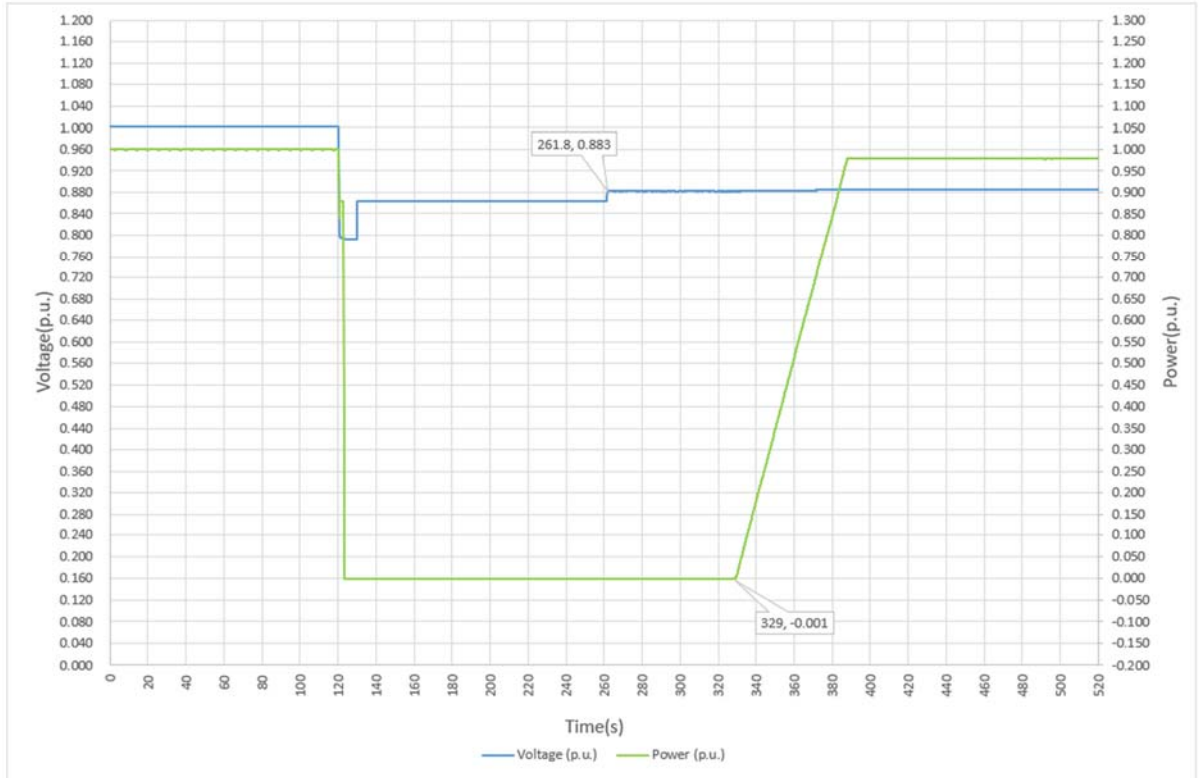
##### 4.5.1 Voltage Reconnection Conditions

The following table detail tests performed.

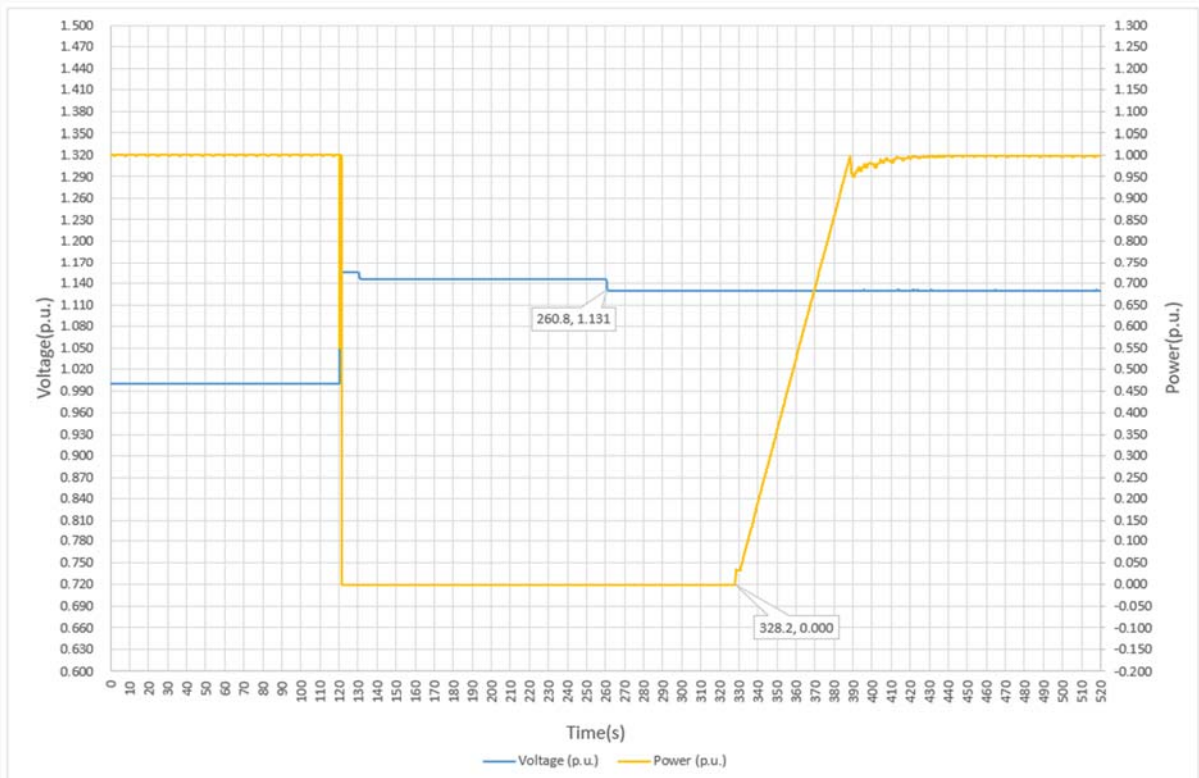
Test at	Time delay setting(s)	Measured delay(s)	Checks on no reconnection when voltage is brought to just outside stage 1 limits of table 1.	
UV	60	67.2	At 466.0V	At 618.5V
OV	60	67.4		
Confirmation that the Micro-generator does not re-connect.			Not reconnection	Not reconnection

Test results are graphically shown below.

**Under voltage reconnection**



**Over voltage reconnection**

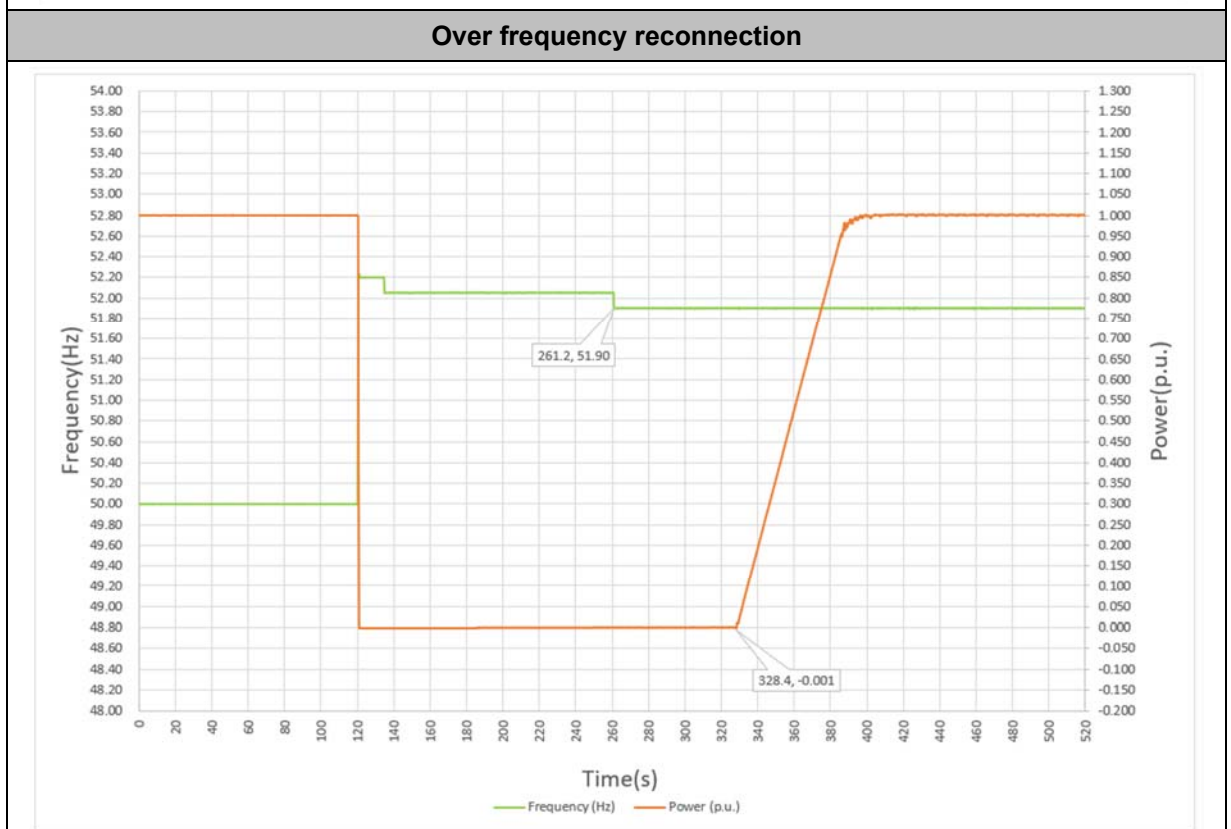
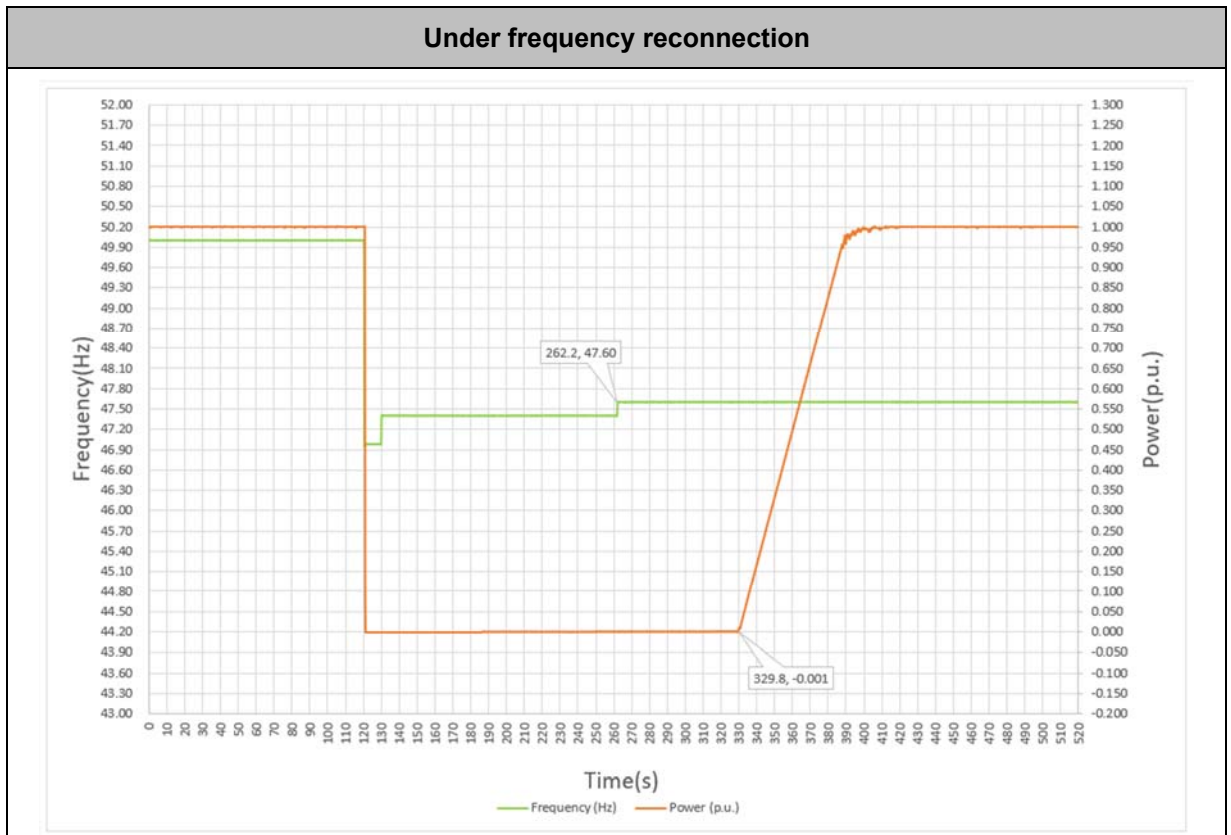


#### 4.5.2 Frequency Reconnection Conditions

The following table detail tests performed.

Test at	Time delay setting(s)	Measured delay(s)	Checks on no reconnection when frequency is brought to just outside stage 1 limits of table 1.	
UF	60	67.6	At 47.4Hz	At 52.1Hz
OF	60	67.2		
Confirmation that the Micro-generator does not re-connect.			Not reconnection	Not reconnection

Test results are graphically shown below.



#### 4.6 Fault level contribution

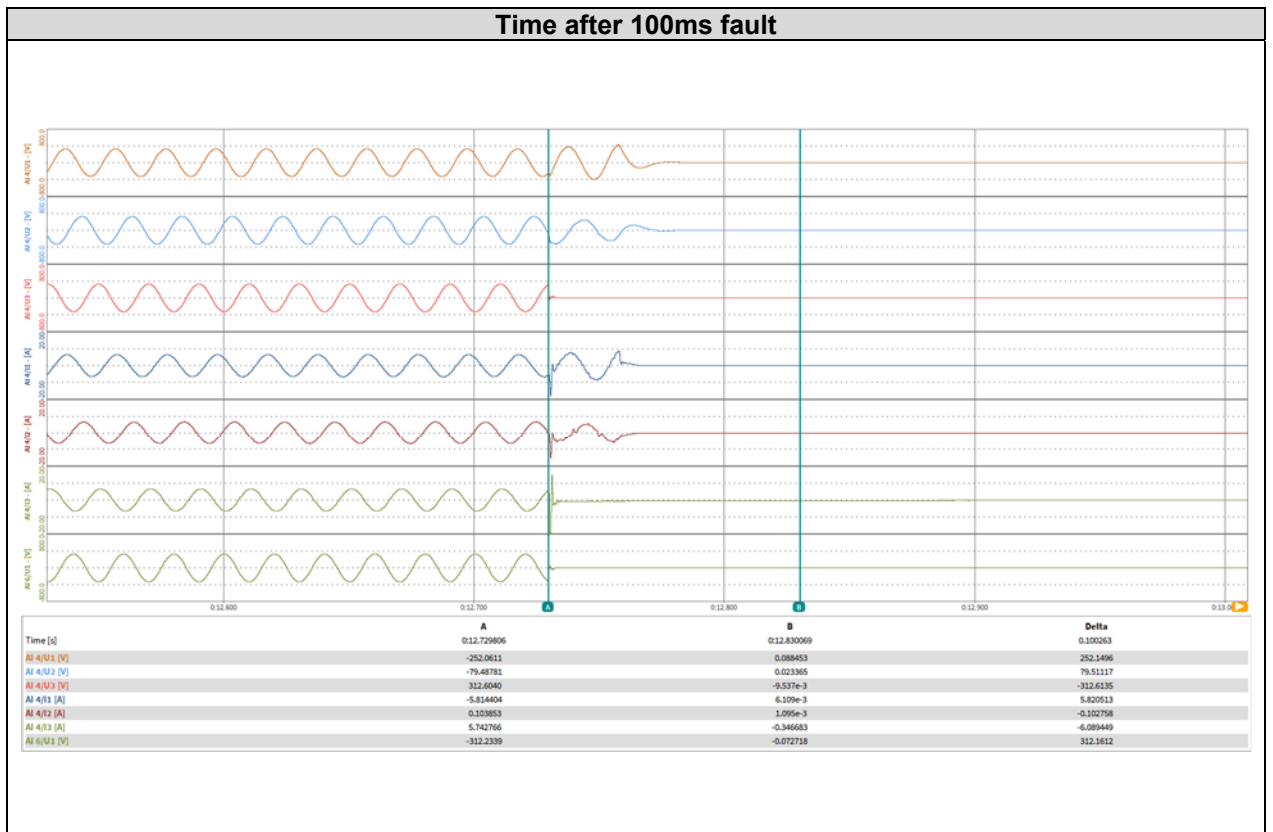
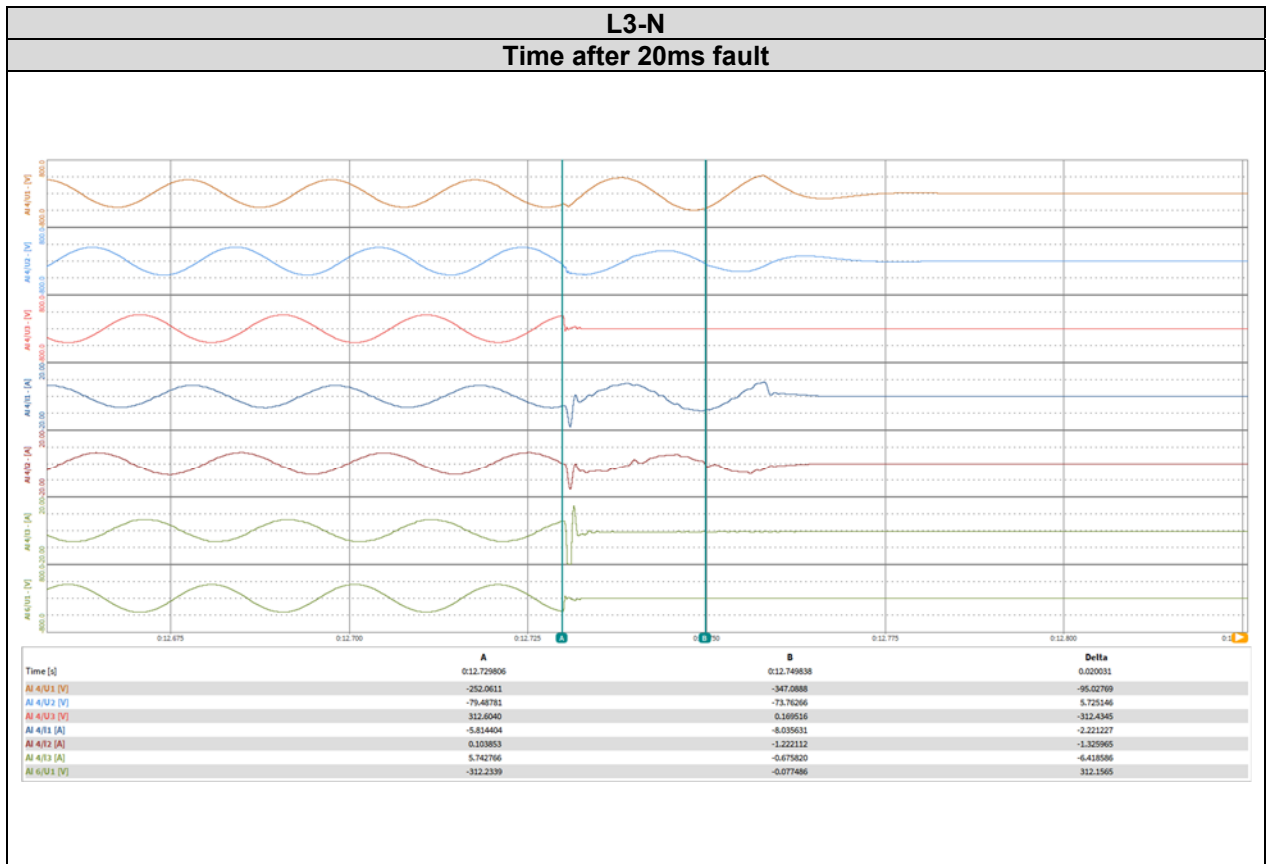
These tests shall be carried out in accordance with EREC G99 Annex A.7.1.5.

They have been performed different short circuit tests that are detailed in the table and pictures below.

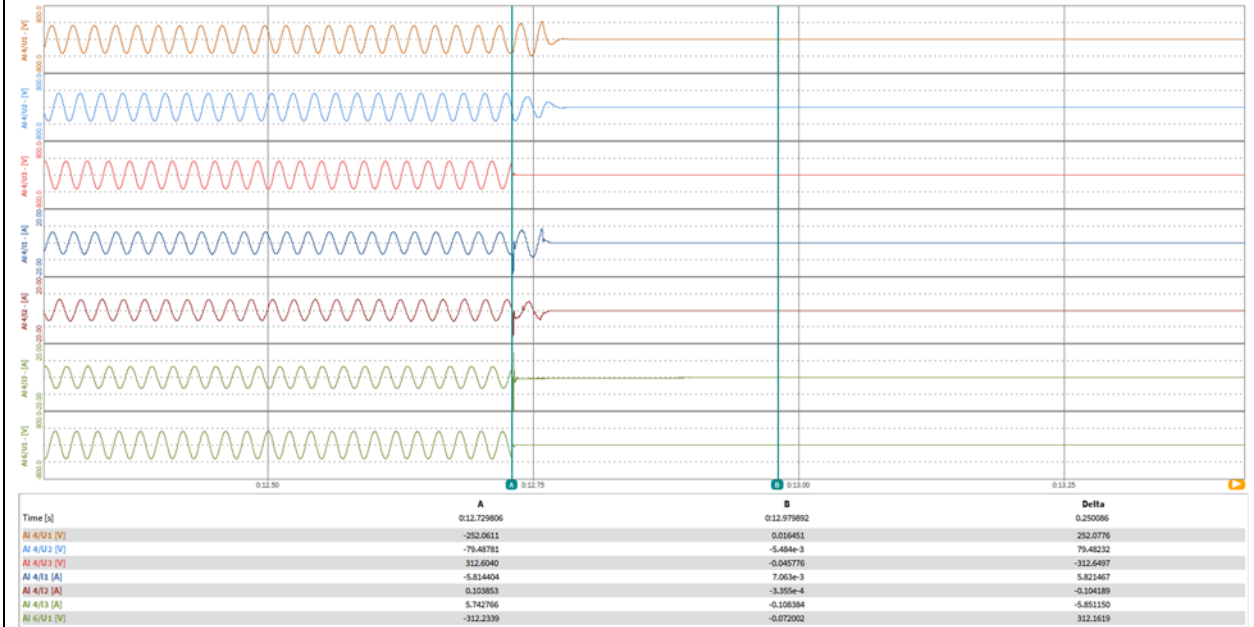
Short circuit current		
L3-N		
Time after fault	Volts(V)	Amps(A)
20ms	347.1	8.0
100ms	0.0	0.0
250ms	0.0	0.0
500ms	0.0	0.0
Time to trip	52ms	In seconds

Short circuit current		
L1-L2		
Time after fault	Volts(V)	Amps(A)
20ms	327.3	7.1
100ms	323.5	7.8
250ms	0.0	0.0
500ms	0.0	0.0
Time to trip	147ms	In seconds

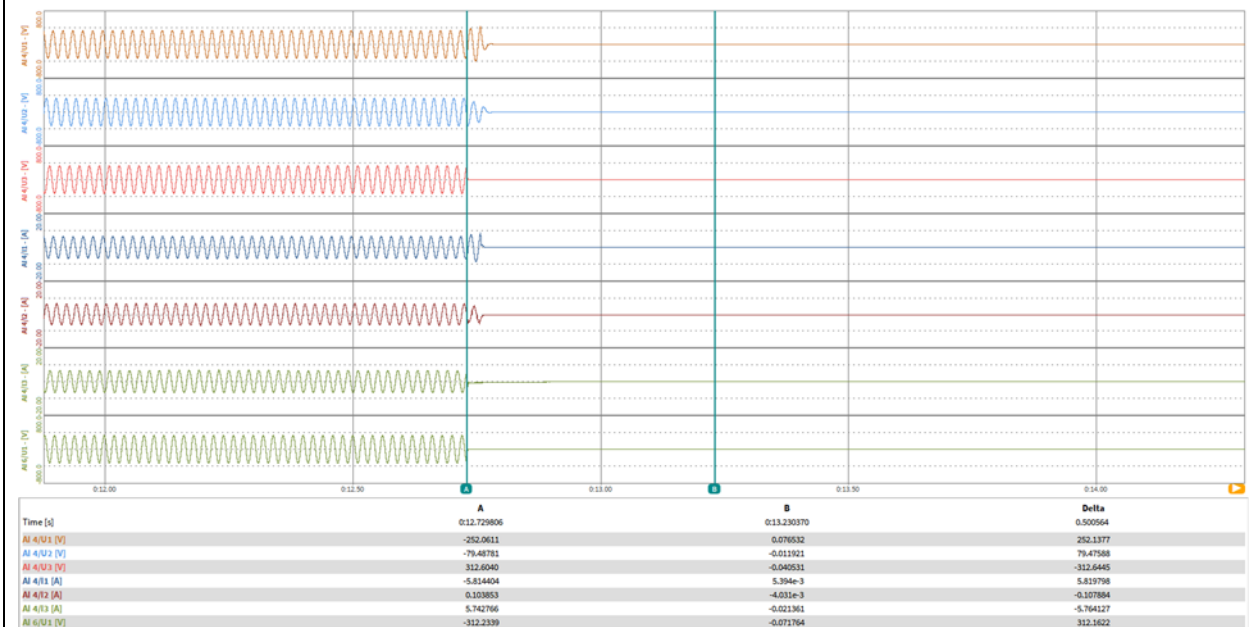


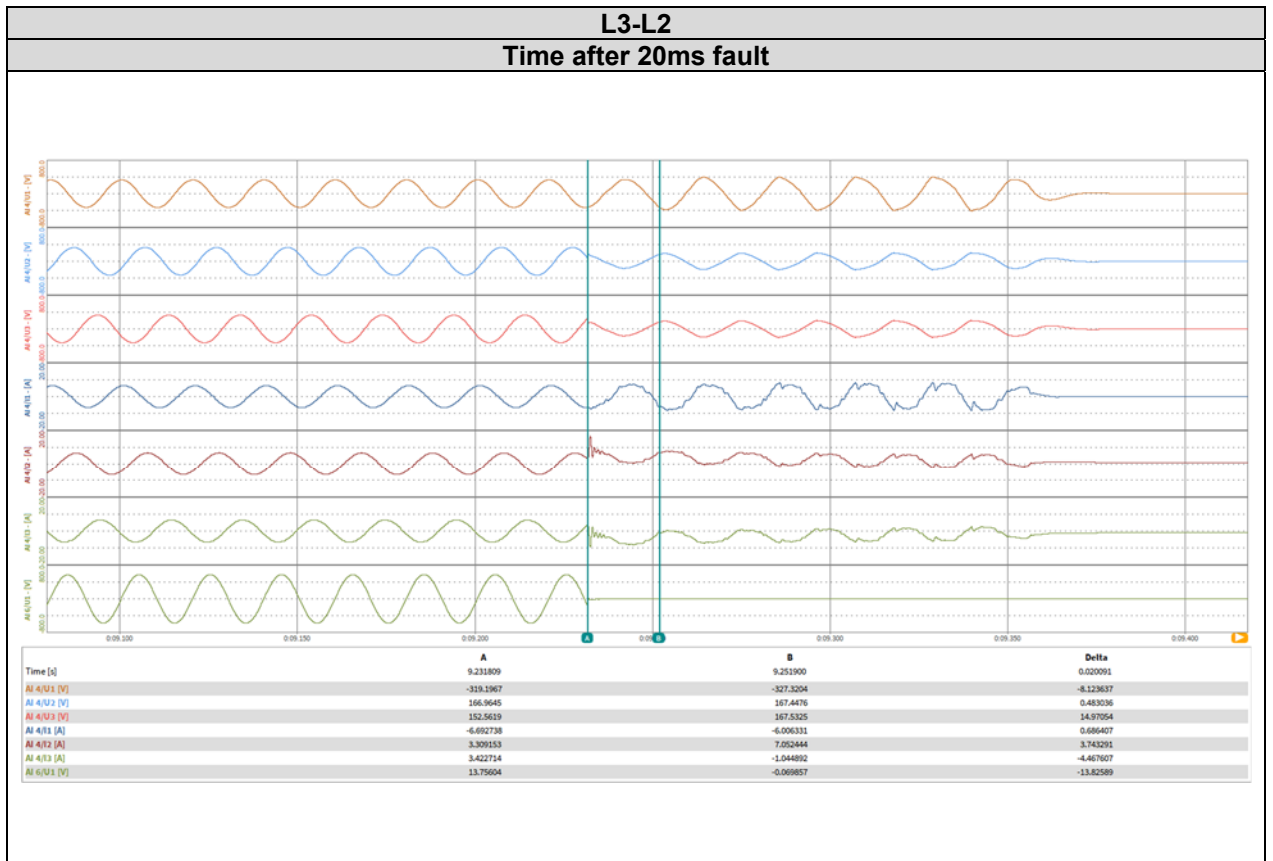
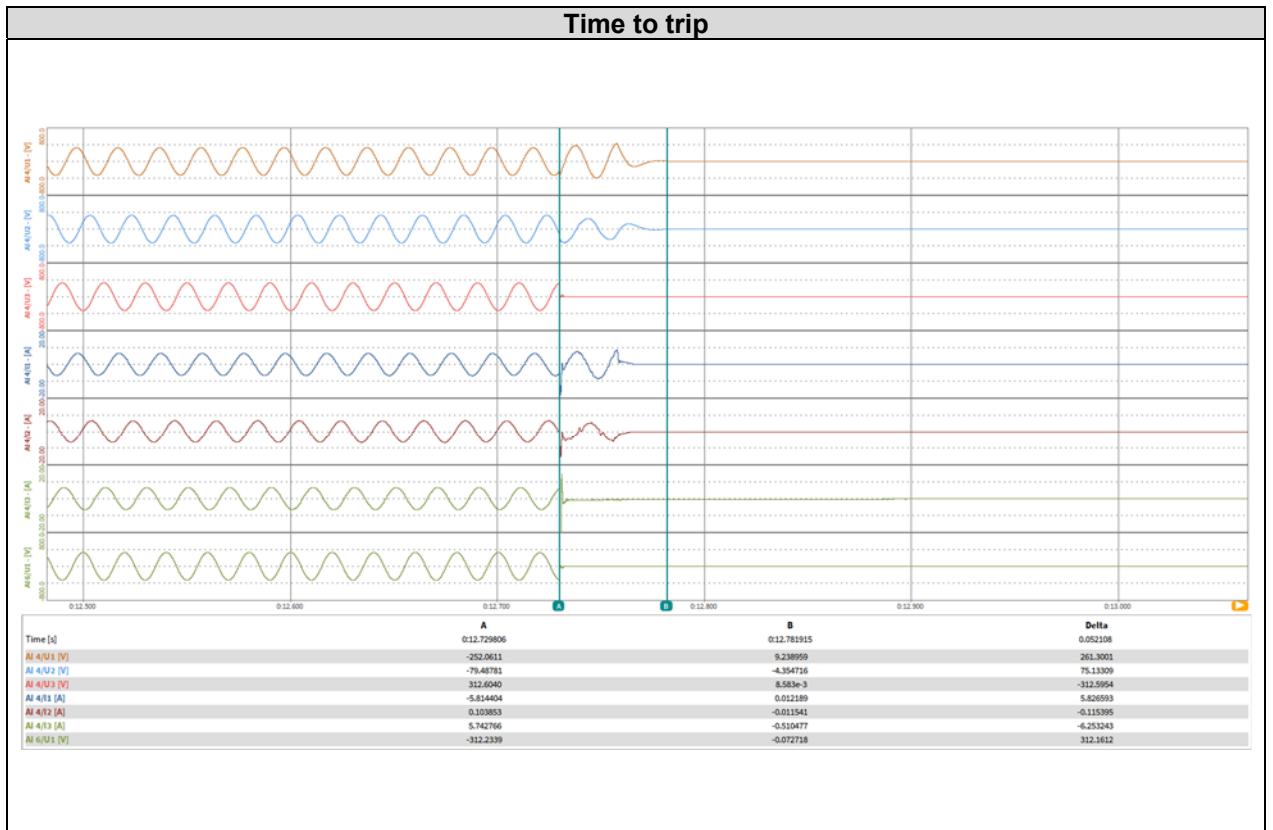


Time after 250ms fault

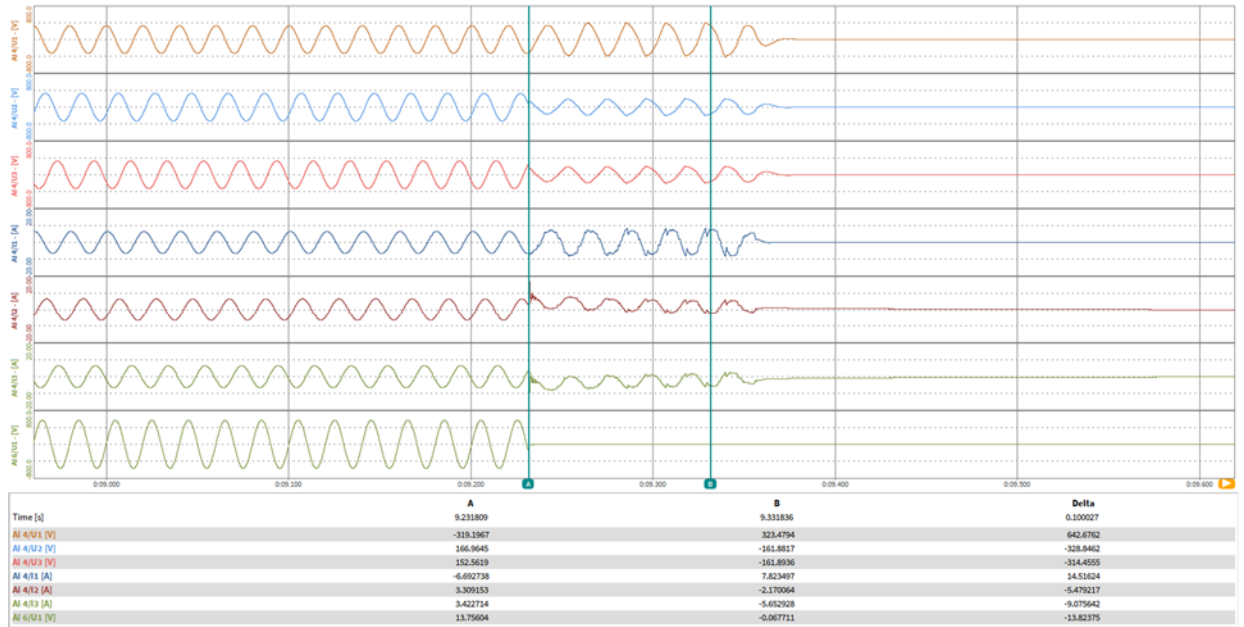


Time after 500ms fault

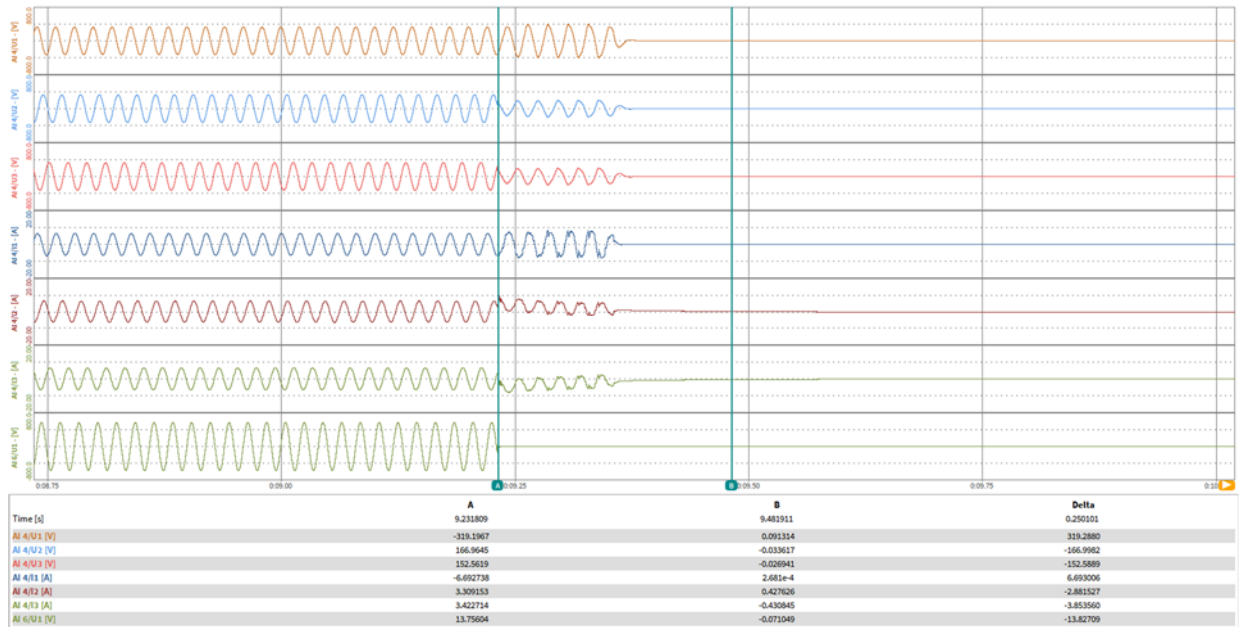




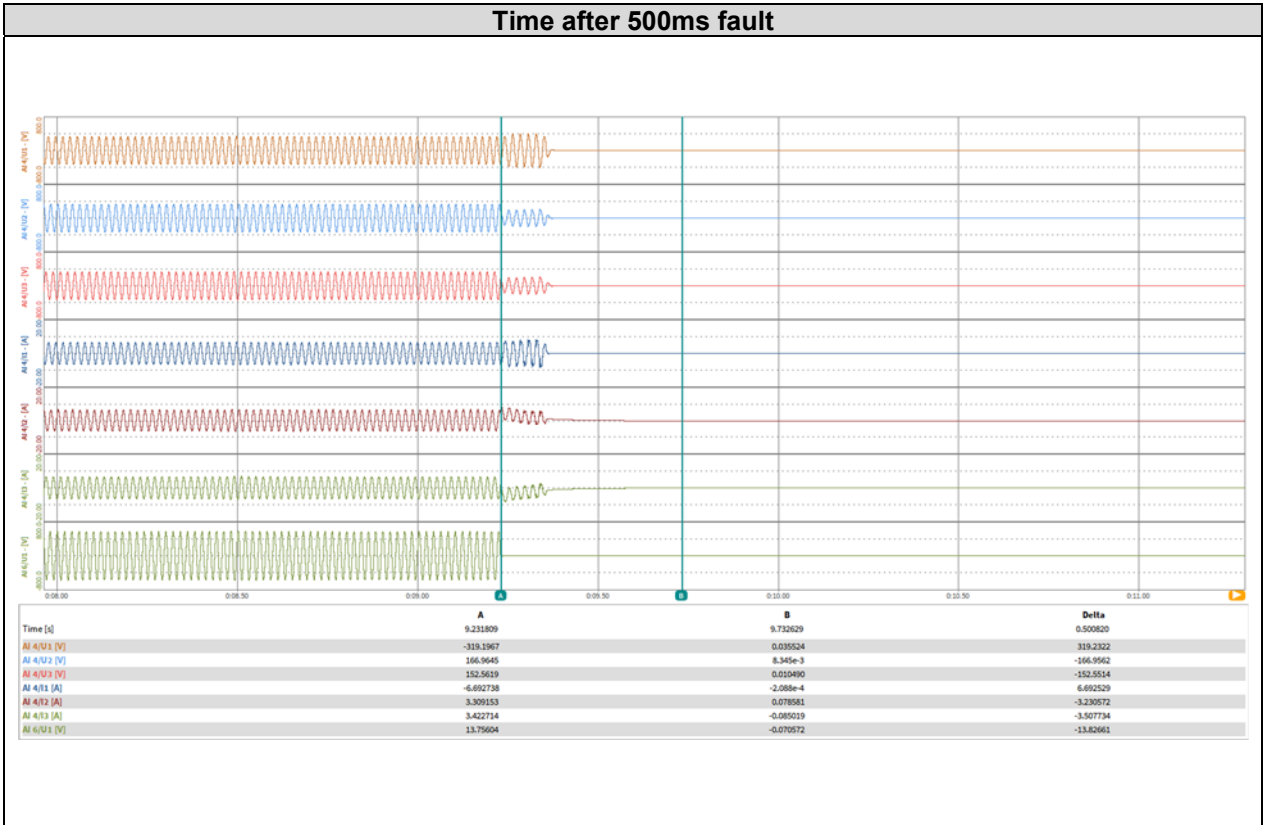
Time after 100ms fault



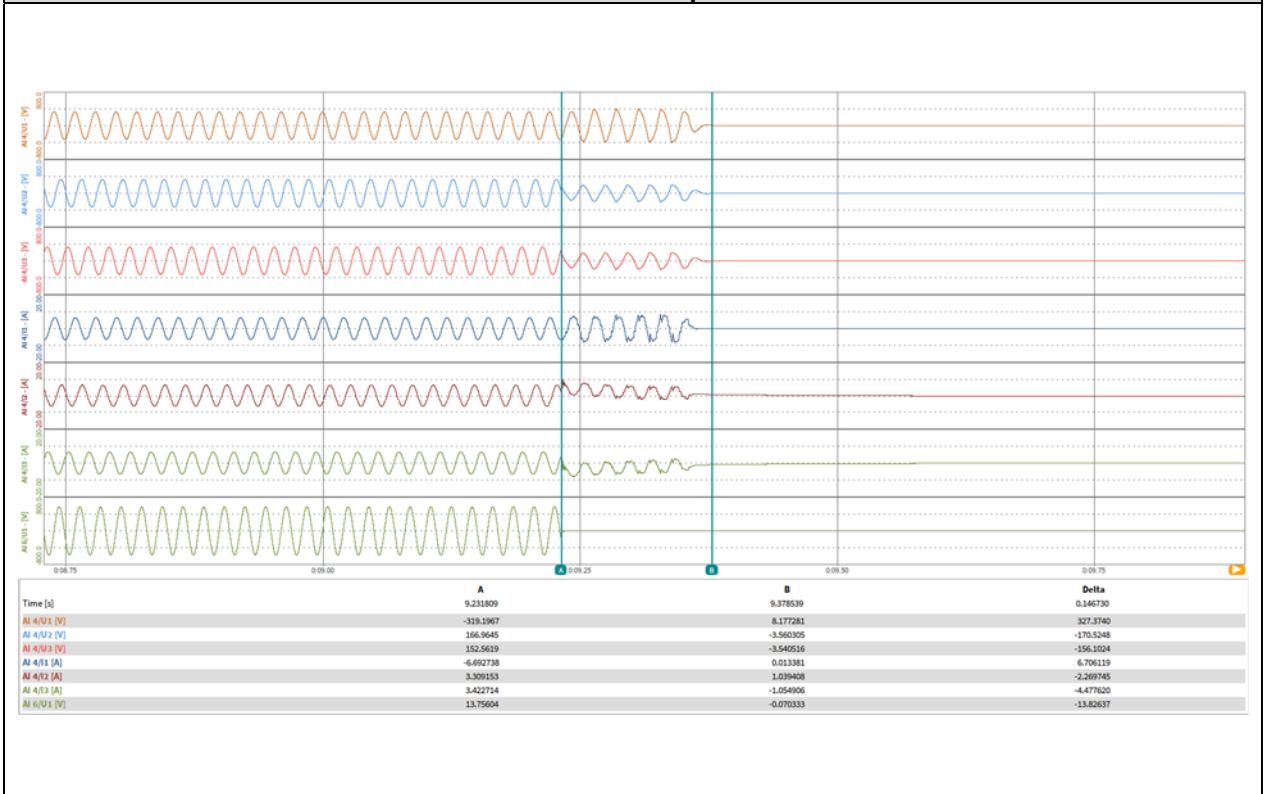
Time after 250ms fault



Time after 500ms fault



Time to trip



#### **4.7 SELF-MONITORING SOLID STATE SWITCHING**

It has been verified that in the event of the solid state switching device failing to disconnect the Power Park Module, the voltage on the output side of the switching device is reduced to a value below 50 volts within 0.5 s.

The evaluation of this point has been made according to Annex A.7.1.7.

This test does not apply because in the inverter there are not solid-state switching devices.

#### **4.8 WIRING FUNCTIONAL TESTS:**

Where Type Tested components are wired together on site, ie not using specifically designed plugs and sockets for the purpose, it will be necessary to prove that all wiring has been correctly terminated by proving the functions which rely on the wiring. The Generator will submit to the DNO for agreement a schedule of the wiring connections to be made, the functions that they enable, and the tests to prove them. Satisfactory completion of the agreed tests will enable the Power Generating Modules to attain or retain Type Tested status.

This test does not apply because connectors were designed error-proof connectors.

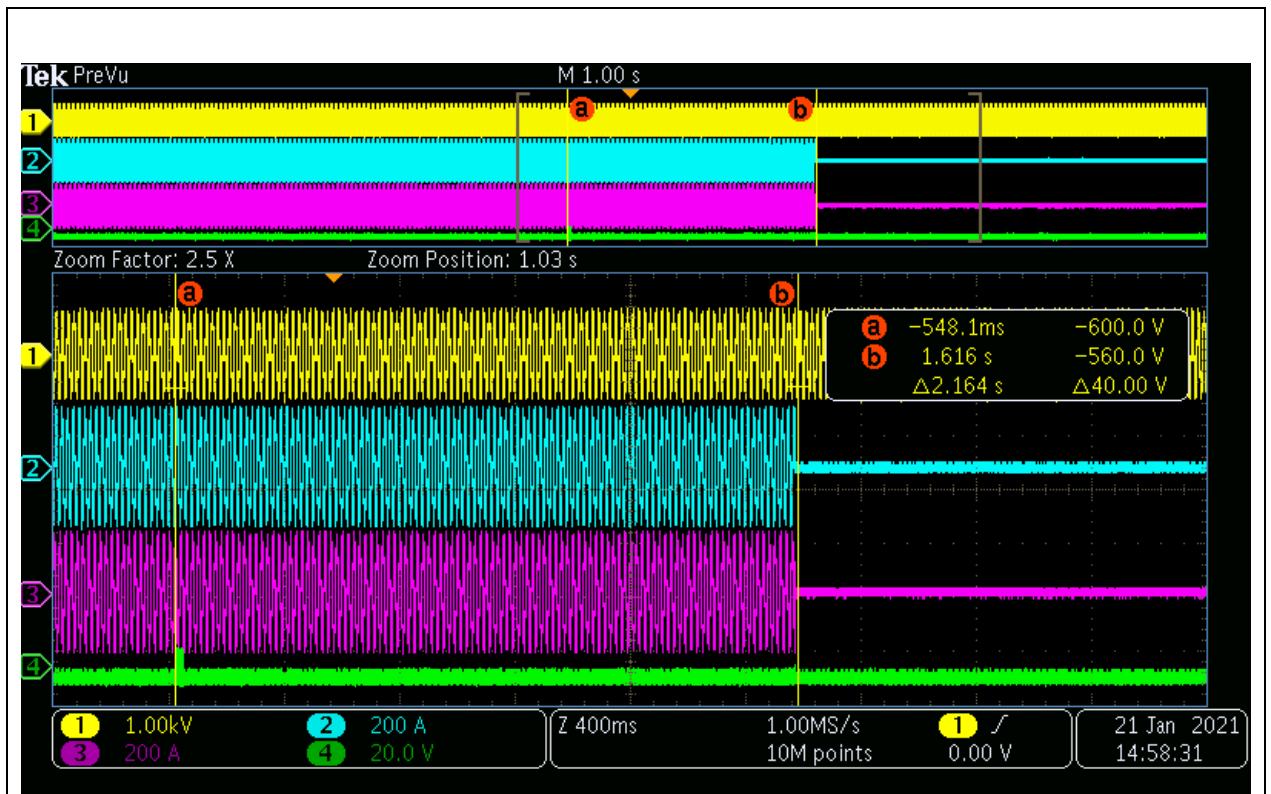
#### 4.9 LOGIC INTERFACE (INPUT PORT).

Confirm that an input port is provided and can be used to shut down the module.

The evaluation of this point has been made according to Clause 11.1.3 of the standard.

Power Generating Modules connected to the DNO's Distribution Network shall be equipped with a logic interface (input port) in order to cease Active Power output within 5 s following an instruction being received at the input port.

Test results are graphically shown as below.



Trip time:2.164s

Ch1: AC Voltage

Ch2 and Ch3: Output Current

Ch4: Signal of logic interface.

5 PICTURES

Front view

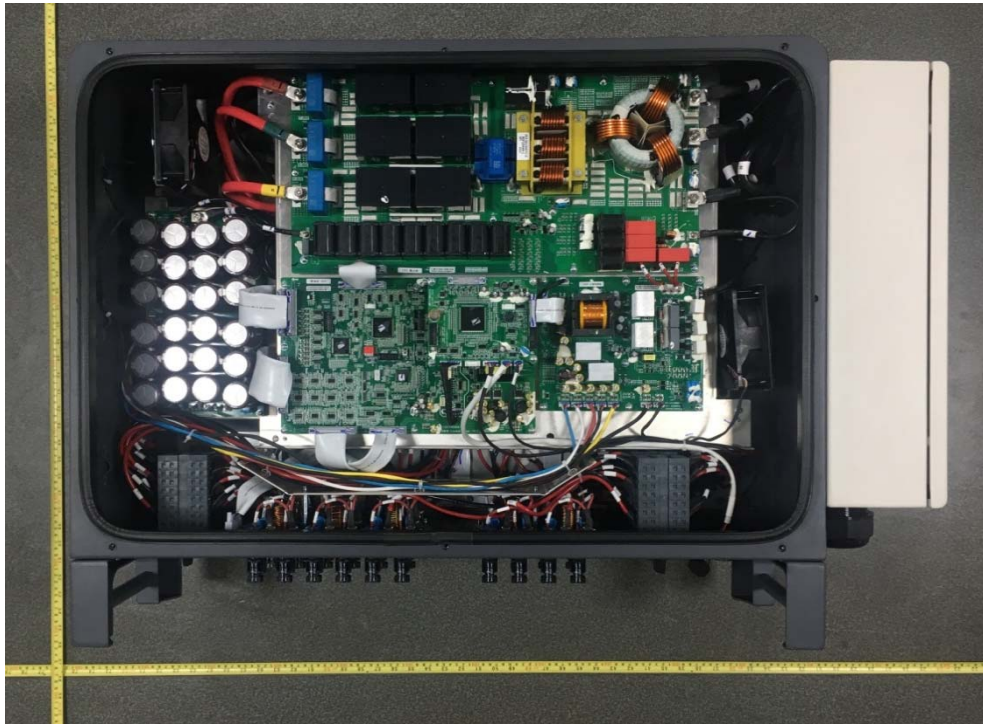


Back view

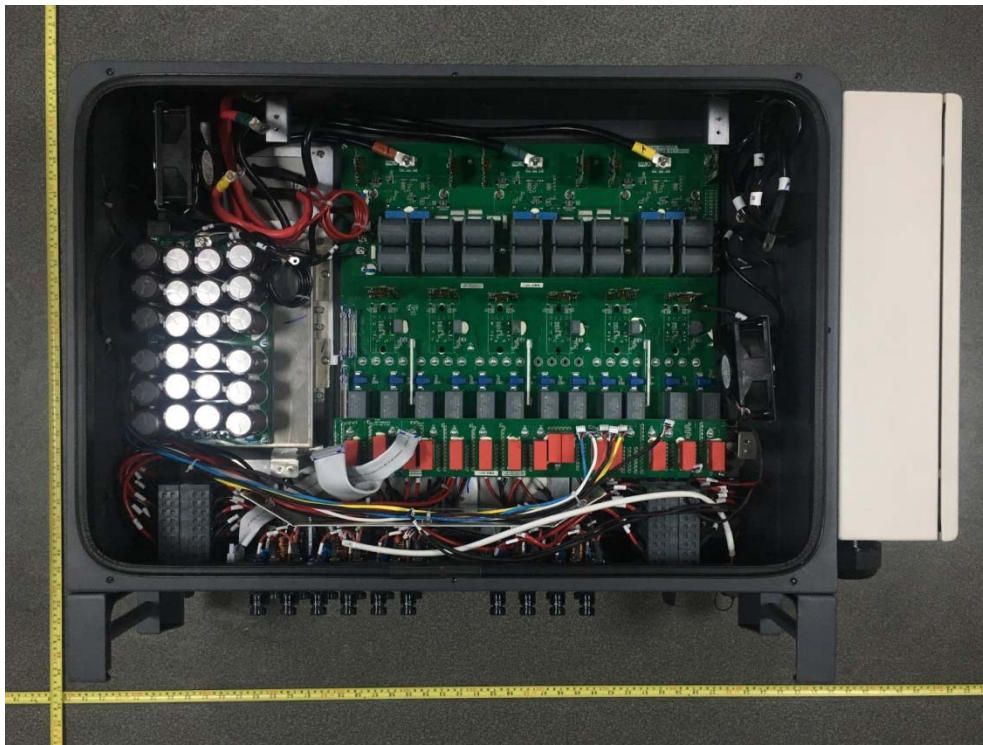




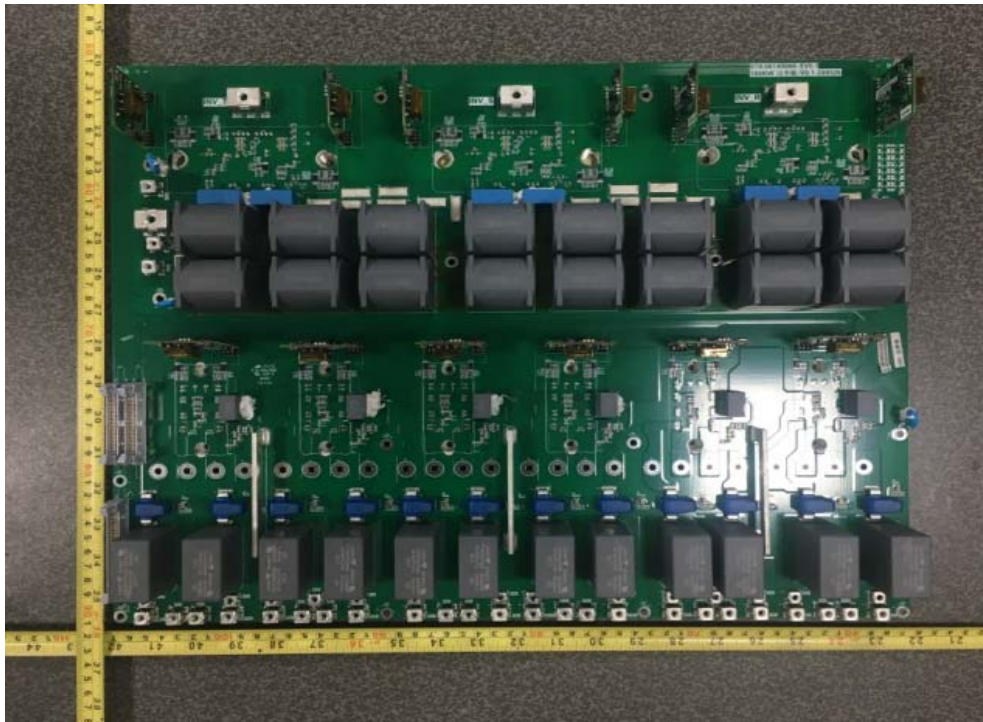
**Internal View 1**



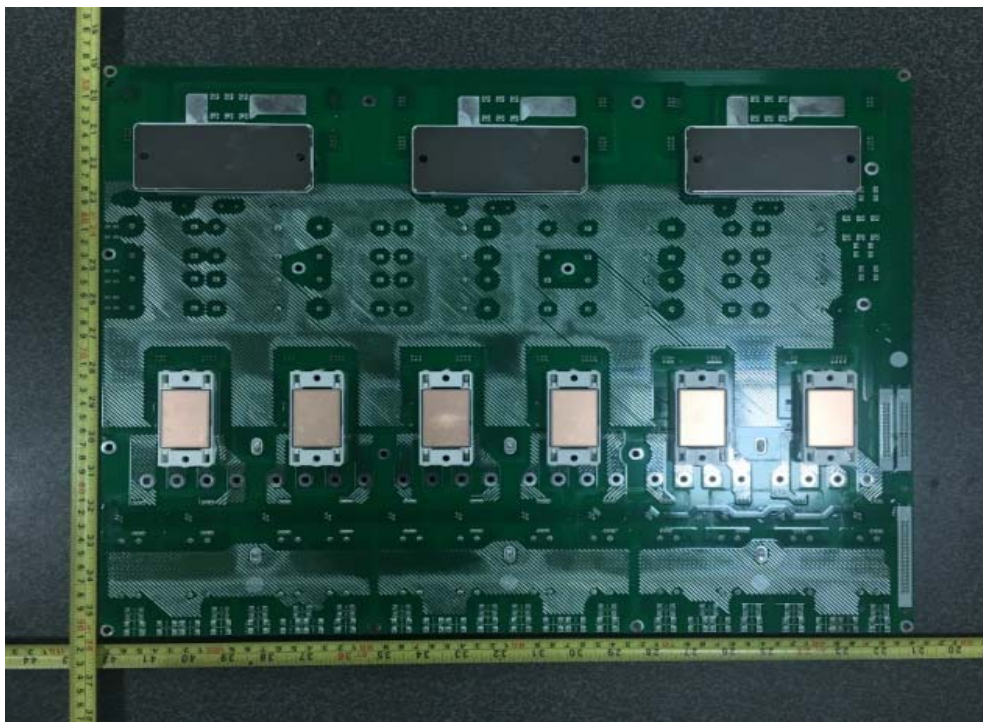
**Internal View 2**



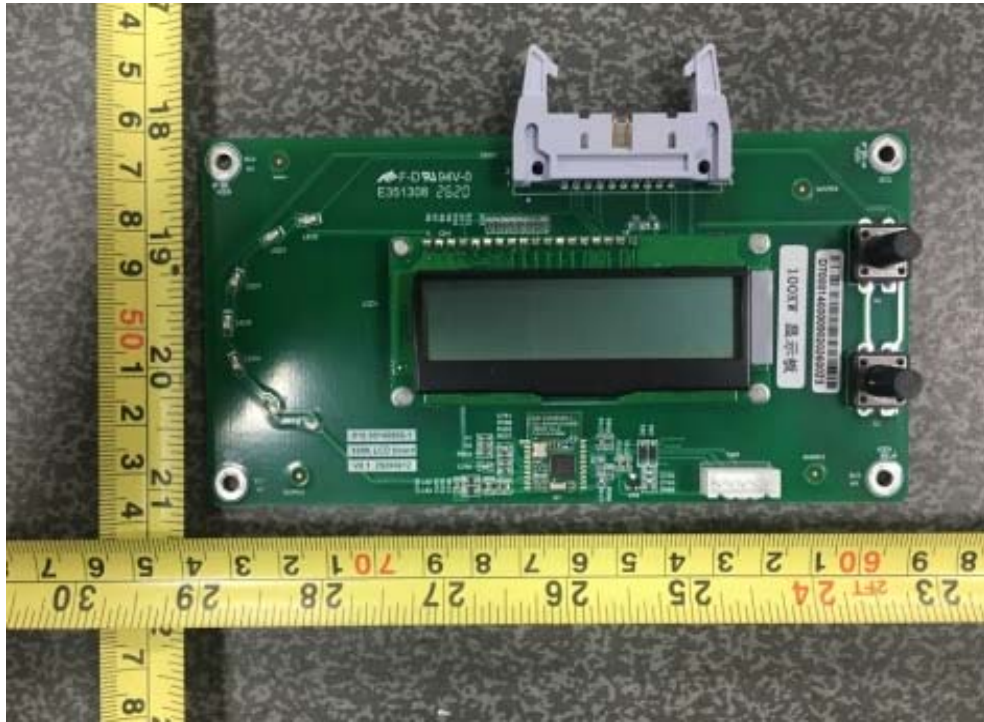
Front side of Power board



Back side of Power board



Front side of Display board



Back side of Display board



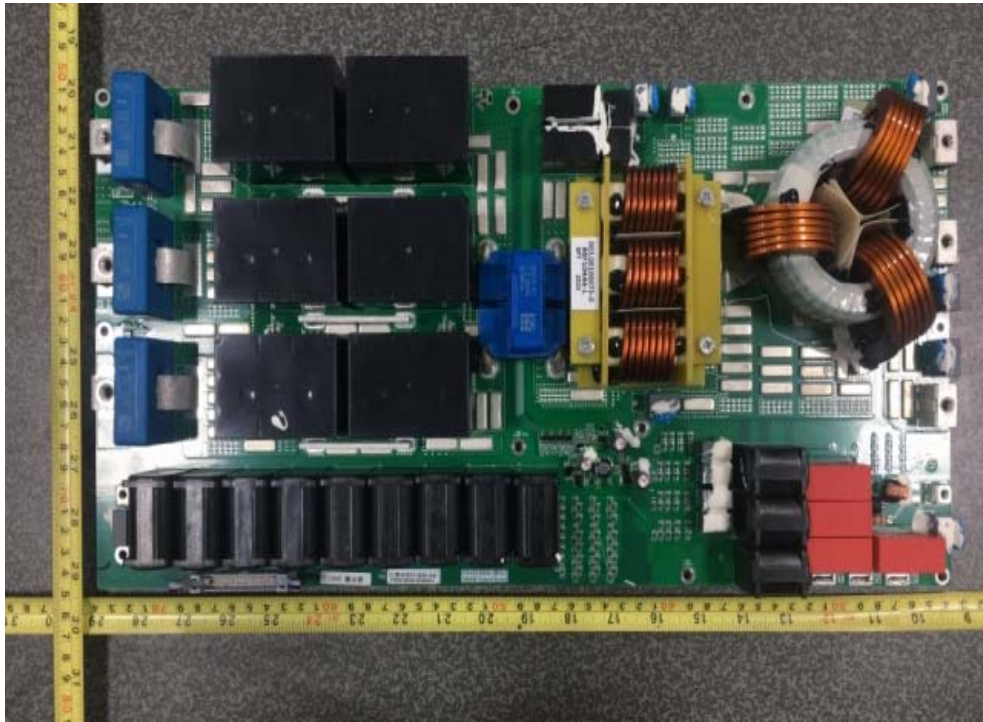
Front side of Control board



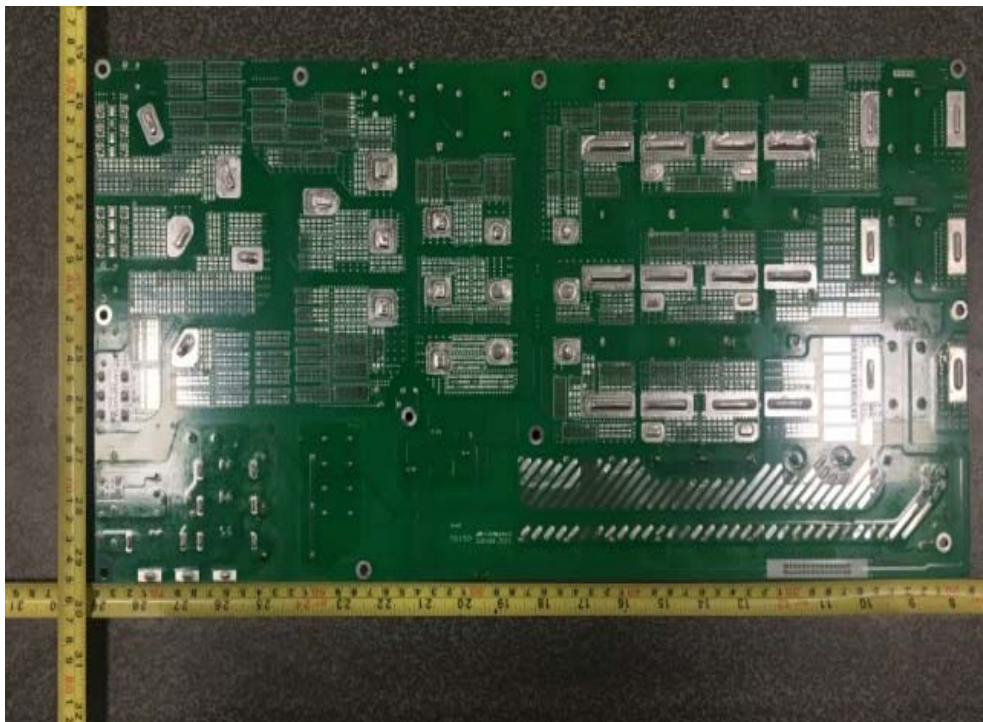
Back side of Control board



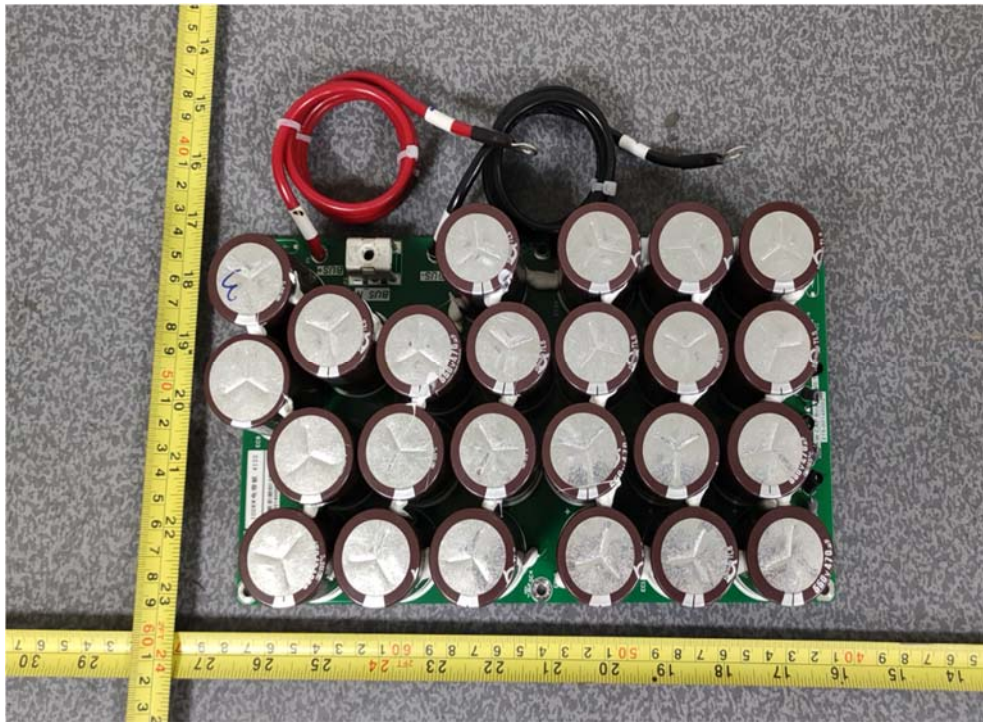
Front side of output board



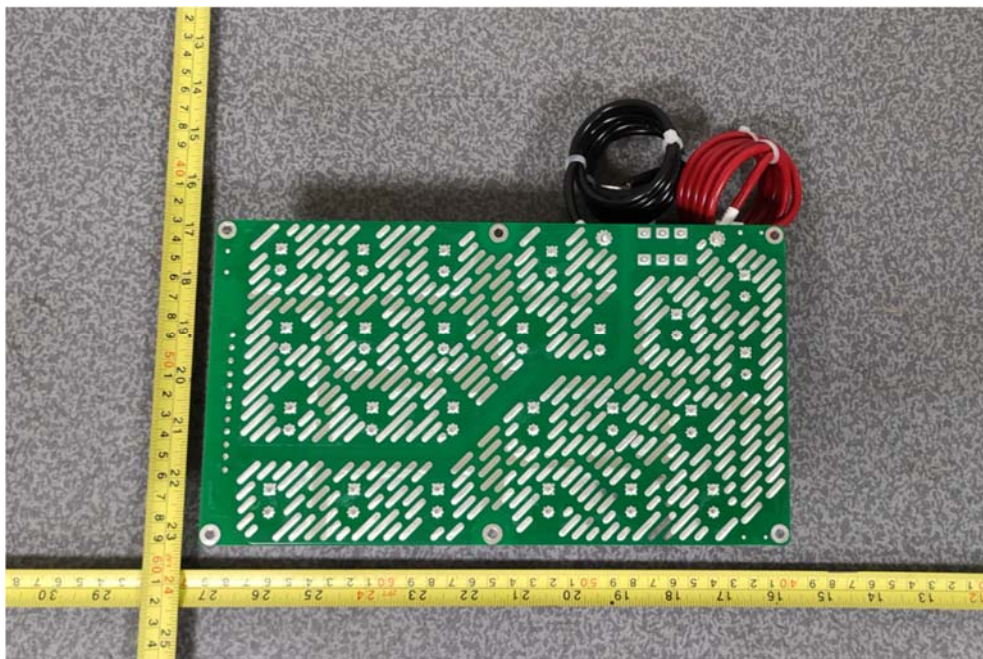
Back side of output board



Front side of BUS Capacitor plate



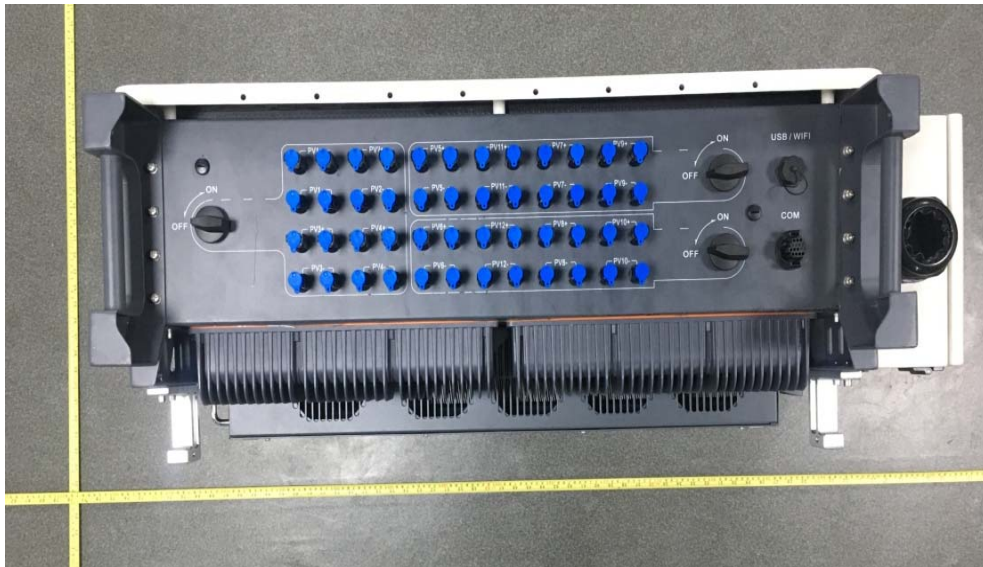
Back side of BUS Capacitor plate



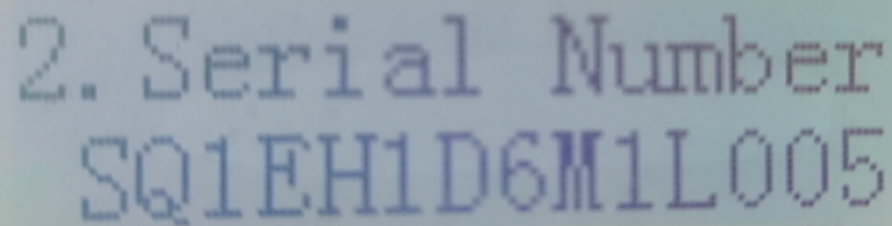
AC Connection interface



DC Connection interface




## Serial number of model




2. Serial Number  
SQ1EH1D6M1L005


## Software Version



3. SoftVersion  
ARM:V020010



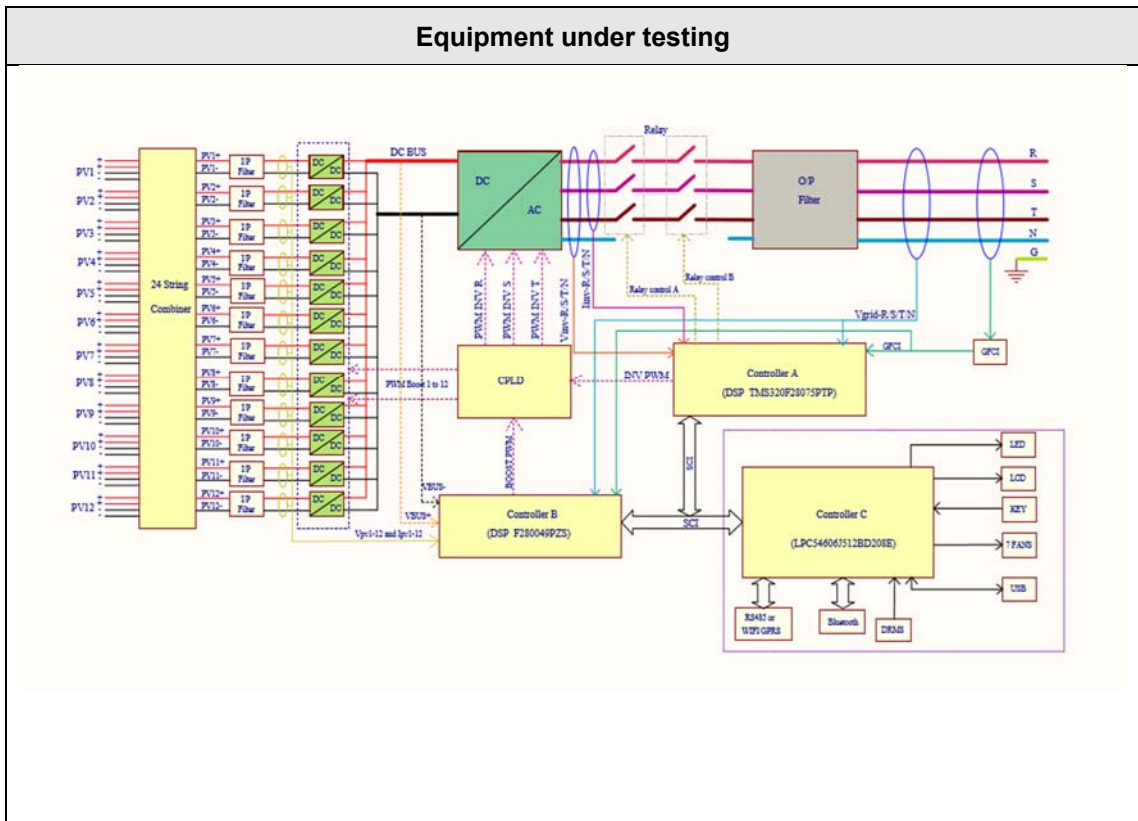
3. SoftVersion  
DSPS:V020010



3. SoftVersion  
DSPM:V020010



6 ELECTRICAL SCHEMES



-----END OF REPORT-----